Vertical GaN Power Transistors Using Controlled Spalling for Substrate Heterogeneity

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Goal: *High performance low cost GaN vertical power devices without re-growth or p-GaN*

Main contents

- GaN Vertical Power FinFET
  - 1st Generation
  - 2nd Generation
  - Benchmarking

- Field-ring trench termination

- Conclusions and Future Work
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Vertical Power FinFET Overview (1)

1st Generation

- Metal-oxide-GaN junction
- Fin width < 300 nm for e-mode operation
- Drift and channel layer: 8 µm 2E16 cm⁻³
- Cap layer: 0.5 µm 4E18 cm⁻³
- No p-GaN/regrowth required
Device fabrication...

- ICP dry etching: Cl₂/BCl₃
- Etch angle ~ 70 deg
- Steep sidewall needed for E-mode

Channel etch

< 500 nm
Written by EBL
Device fabrication...

For steep sidewall, channel ‘fins’ aligned to a-plane
Device fabrication…

Gate dielectric: 15nm ALD Al₂O₃
Gate metal: sputtered Mo

Coating with photoresist

Etch gate oxide/gate metal
Device fabrication...

PECVD oxide as gate/source spacer

Ti/Al as drain/source metal

1st Generation
Device fabrication…

source

Channel

Gate

SiO$_2$ spacer

450 nm

500 nm
Transfer characteristics

$I_{on}/I_{off} \sim 10^{11}$

$V_{th} \sim 1.0 \text{ V @ on/off} = 10^5$

Subthreshold swing $\sim 75 \text{ mV/dec}$

Minimum hysteresis

Channel width = 180 nm

$V_{th} = V_{bi} - qN_0W^2/8\varepsilon_s$

$V_{th}$ defined at $I_{DS} = 10^{-3}$ A/cm$^2$

Oxide interface charge: $\sim 9 \times 10^{11}$ cm$^{-2}$
Output Characteristics

Channel width = 180 nm

- $V_{GS,max} = 5 \text{ V}$
- $V_{step} = -1 \text{ V}$

- $R_{on} \sim 0.36 \text{ mΩcm}^2$
- Normalized by the active channel area
Output Characteristics

- Transistor area: $0.8 \times 0.8 \text{ mm}^2 = 0.64 \text{ mm}^2$
- Highest current density $\sim 9\text{A}$ at $V_{GS} = 5\text{ V}$
- Fin width: $0.25 \mu\text{m}$
- Active area: $0.09 \text{ mm}^2$

<table>
<thead>
<tr>
<th></th>
<th>Active area</th>
<th>Total area</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current density (kA/cm$^2$)</td>
<td>~10</td>
<td>~1.4</td>
</tr>
<tr>
<td>On resistance (m$\Omega$cm$^2$)</td>
<td>0.9</td>
<td>6.4</td>
</tr>
</tbody>
</table>
Breakdown voltage (1)

Gate field plate

Insulating oxide layer

1st Generation

$V_{GS} = 0$

$V_{DS}$ (V)

$I_{DS}$ (A/cm$^2$)

$10^{-1}$

$10^{-2}$

$10^{-3}$

$10^{-4}$

$10^{-5}$

$10^{-6}$

$10^{-7}$

$0$  $100$  $200$  $300$  $400$  $500$

w/o fp

w/ fp
Breakdown voltage (2)

Oxide spacer

gate

oxide

channel

source

220 nm

730 nm

100 nm
Breakdown voltage (3)

- \( BV > 800 \, \text{V} \) @ \( V_{GS} = 0 \, \text{V} \)
- Peak electric field in the drift region \( \sim 2.5 \, \text{MV/cm} \)
Pulsed measurement

\[(V_{G,q}, V_{D,q}) = (0,0), V_G = 4 \text{ V}; \text{ duty ratio} = 0.5\%;\]

- Limited dynamic $R_{on}$ increase
- More work needs to be done at higher voltages
Improved ON resistance (1)

• Annealing temperature is limited at 400ºC: higher temperature will significantly increase the gate leakage current
Improved ON resistance (1)

- Annealing temperature is limited at 400°C: higher temperature will significantly increase the gate leakage current
- In Gen. 3 devices, cap layer doping increased from $4 \times 10^{18}$ cm$^{-3}$ to $1 \times 10^{19}$ cm$^{-3}$
- IV of source contact changes from ‘Schottky’ shape to Ohmic
- Ohmic contact resistance: $\sim 4.5 \times 10^{-5}$ Ωcm$^2$

Both annealed at 400 °C
Improved ON resistance (2)

Fin width = 250 nm

\[ V_{th} = 0.79 \text{ V} \quad @ \quad I_{on}/I_{off} = 10^5 \]

SS = 80 mV/dec

\[ R_{on} = 0.089 \text{ m}\Omega\text{cm}^2 \]

(normalized to fin width)

(vs \( R_{on} = 0.36 \text{ m}\Omega\text{cm}^2 \) in Gen2 devices)
Improved ON resistance (3)

Source ohmic contact: 0.045 mΩcm²

Access region resistance: 0.01 mΩcm²

Channel resistance: 0.005 mΩcm²

Drift layer: 7 µm, 2×10^{16} cm⁻³; \( R_{\text{drift}} \sim 0.21 \) mΩcm²

Consider current spreading and normalized to fin area: 0.009 mΩcm²

Sub: 400 µm, 2×10^{18} cm⁻³; \( R_{\text{substrate}} \sim 1.3 \) mΩcm²

Consider current spreading and normalized to fin area: 4.8×10⁻⁴ mΩcm²

Drain back contact much larger than the intrinsic DUT: current spreading
Improved ON resistance (4)

Drain contact has a similar size than the device after dicing

Resistance components for a complete vertical GaN transistor

Specific ON resistance $R_{on} = 1.74 \text{ m$\Omega$cm}^2$ for a ‘diced’ vertical GaN transistor
Improved ON resistance (5)

How to further reduce $R_{on}$?

Future device if we thin down substrate

SWITCHES target 3 mΩcm$^2$

This work

Si

4H-SiC

GaN

$V_{BR}$ (V)

$R_{on,sp}$ (mΩcm$^2$)
For more details: S. Bedell’s talk today at 1:50pm
Spalling Technology

Preliminary results on spalled diodes: Much better forward IV after spalling

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Advanced GaN Field Termination

- Motivation
  - Need field termination to further increase transistor breakdown

- Approach
  - Ion implantation between fin structures to engineer electric field
Advanced GaN Field Termination

- **Motivation**
  - Need field termination to further increase transistor breakdown

- **Approach**
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- **Demonstration vehicle:** GaN Vertical field-ring (FR) Trench MIS Barrier Schottky (TMBS) Rectifiers
  - (a) lateral depletion by MIS, lowering E-field at Schottky
  - (b) Trench FR: deeper termination into bulk GaN
Advanced GaN Rectifiers (1)

- E-field at Schottky interface greatly reduced
- Peak E-field moves from Schottky interface into bulk GaN
- E-field crowding in dielectrics in TMBS, solved by inserting FRs

Y. Zhang et al., IEDM 2016
Advanced GaN Rectifiers (3)

- FR-TMBS: 100-fold lower leakage: BV: 500 V -> 700 V
- Peak E-field moved into bulk GaN
- Leakage Mechanism: VRH + SCLC, similar to pn diodes, Schottky-like forward characteristics: $V_{on}: 0.7-0.8$ V; $R_{on}: 2\sim3 \text{ m}\Omega \cdot \text{cm}^2$
- High-temperature (>200 C) operation
- Currently transferring this technology to vertical power FinFETs (Gen. 4)
Future work

- Optimize spalling to reduce substrate access resistance.
- Increase breakdown voltage in Gen. 4 devices by:
  - Reducing doping in drift region.
  - Optimizing field rings between fins
- Fabrication of large area devices with Gen. 4 technology
- Additional studies of long term stability and reliability in transistors
- Custom packaging (see Prof. Shepard’s talk on Wednesday)
Technology-to-Market

- Vertical Power FinFET and field-management technologies have been patented.
- Currently looking for companies interested in licensing transistor technology.

Challenges:
- Quality/reproducibility of bulk GaN wafers is still an issue
- Need to understand long-term stability
Conclusions

- New vertical GaN transistor technology demonstrated
- Extremely high current densities possible
- Field management in the trench is critical for high breakdown voltage
- Initial stability measurements are promising
- Wafer spalling critical to reduce substrate resistance in a cost-effective manner