Ultra-energy-efficient integrated DWDM optical interconnects for future HPC systems

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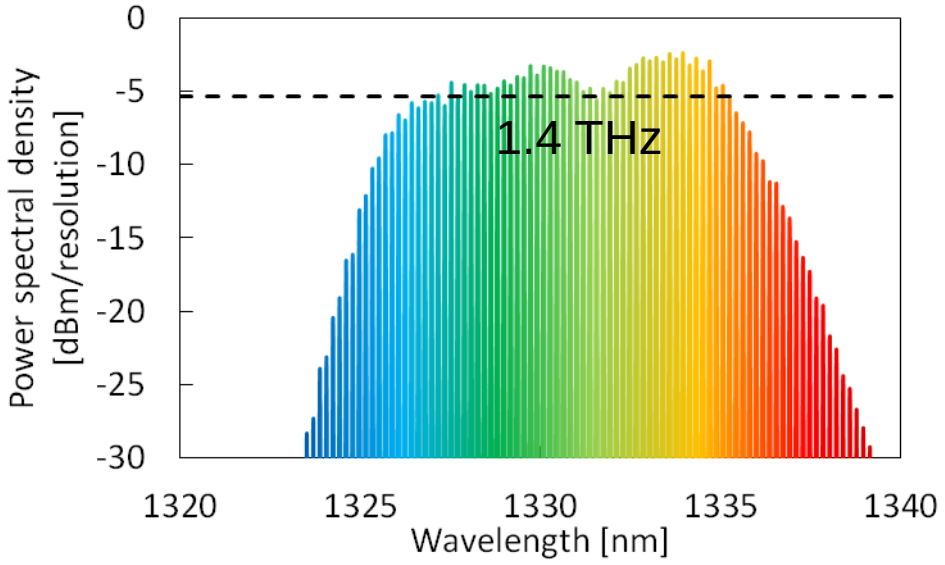
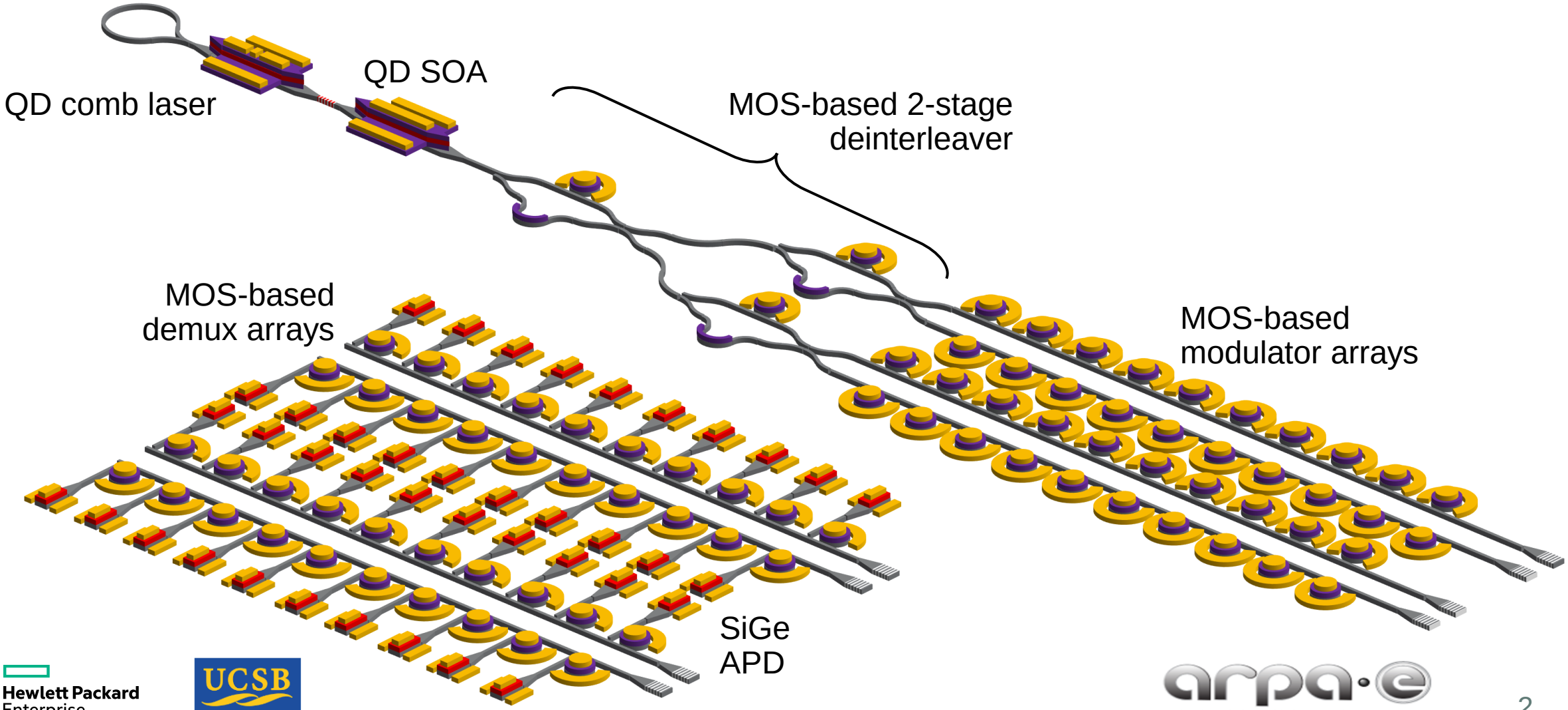


Program Goal: >1 Tb/s, <1.5 pJ/b* link with FEC-free BER ≤ 10^{-9} at 50°C
*Laser, SOA, modulator, tuning of optical components, APDs



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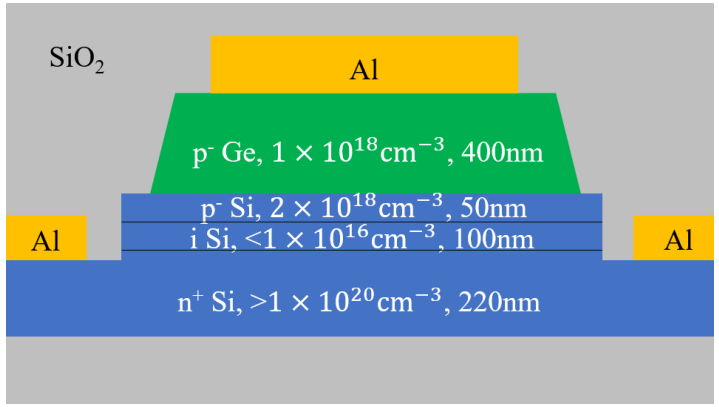
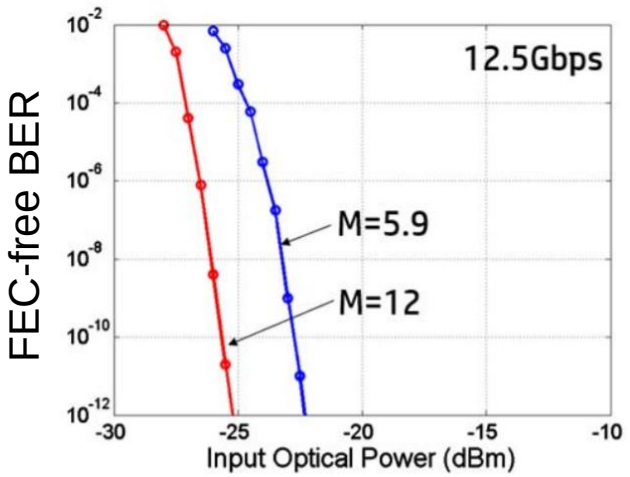
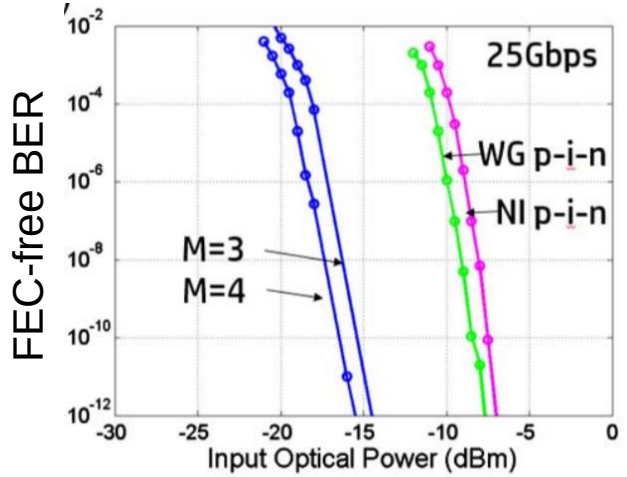
SiGe APDs

– Gain in photodetector → better sensitivity → can drive laser at lower drive current → energy savings







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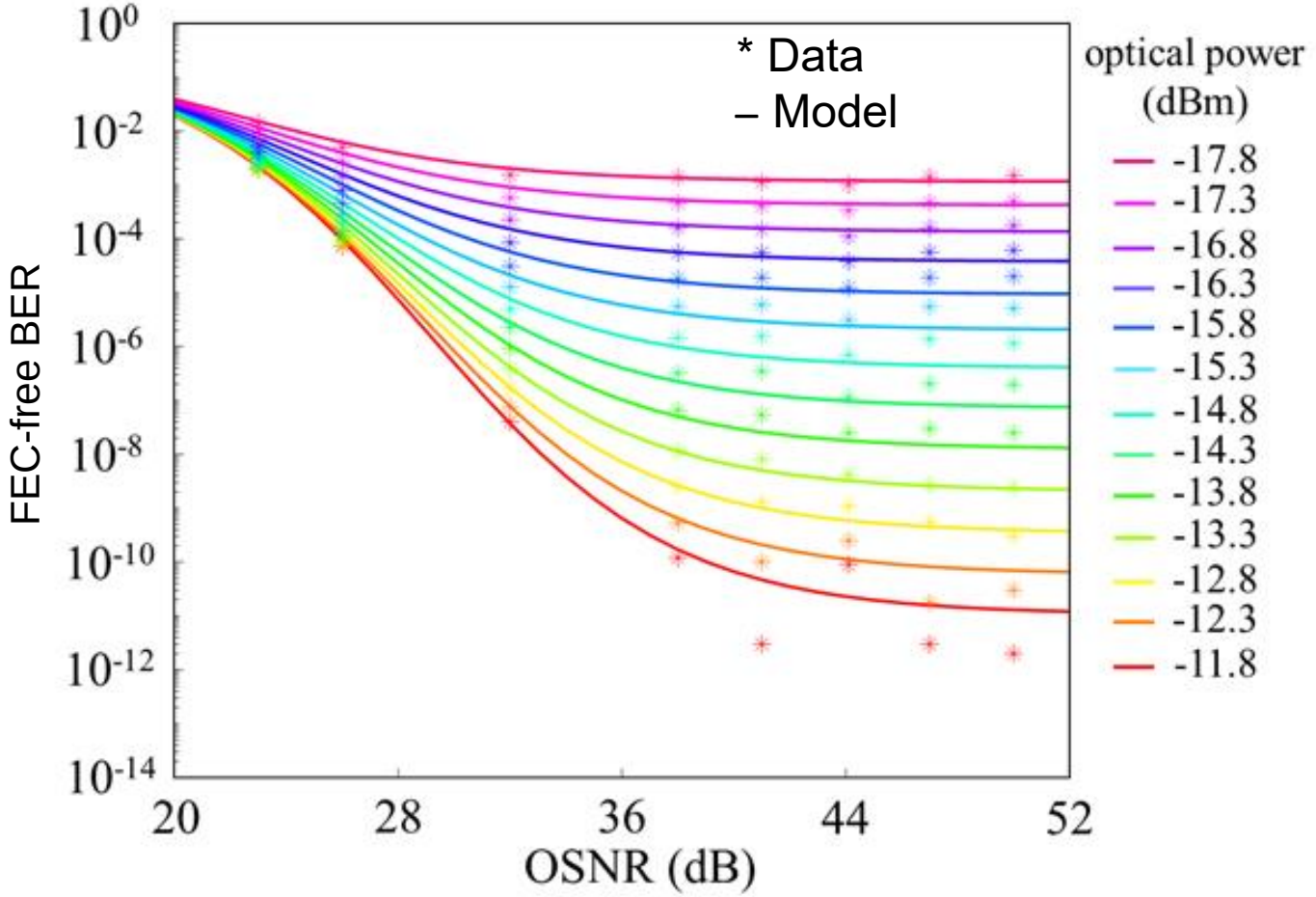
SiGe APDs



– Need OSNR ≥ 36 dB for FEC-free BER ≤ 10^{-9}
  – HPC favors FEC-free BER ≤ 10^{-12} because of latency

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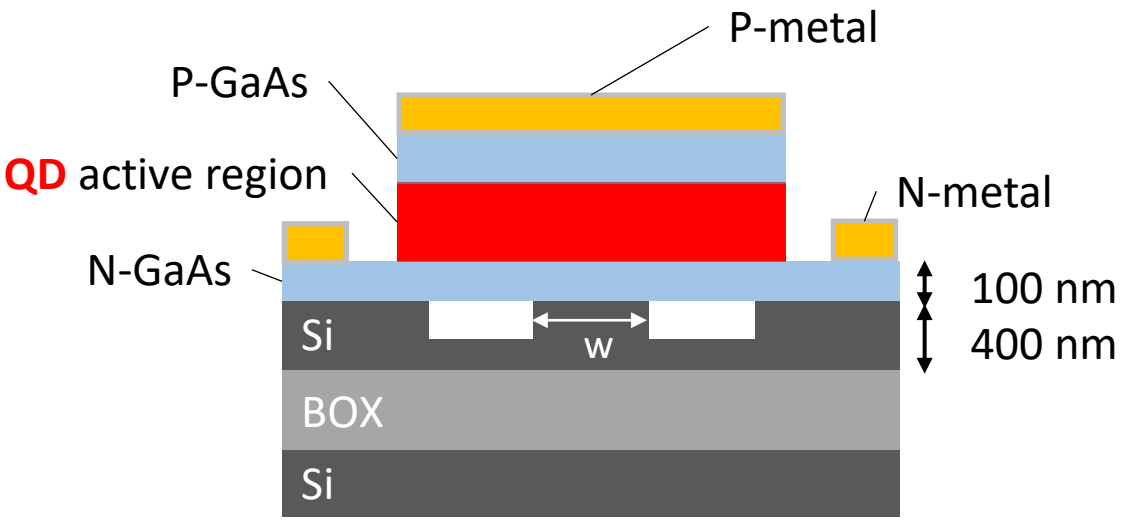
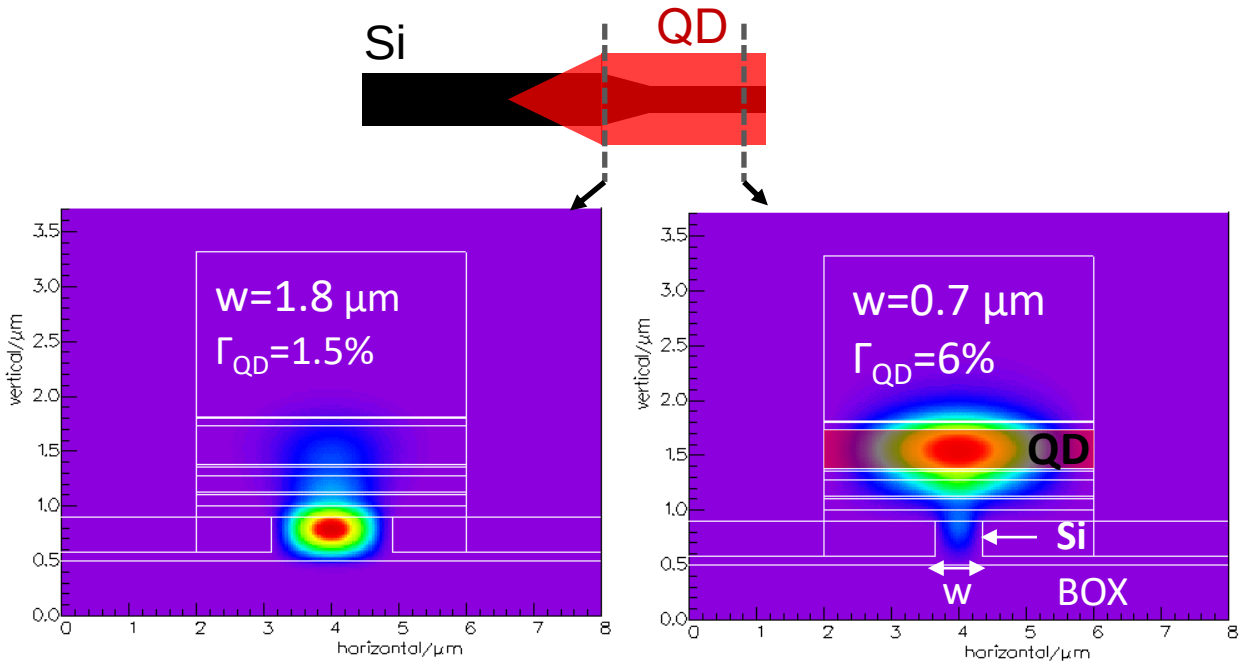
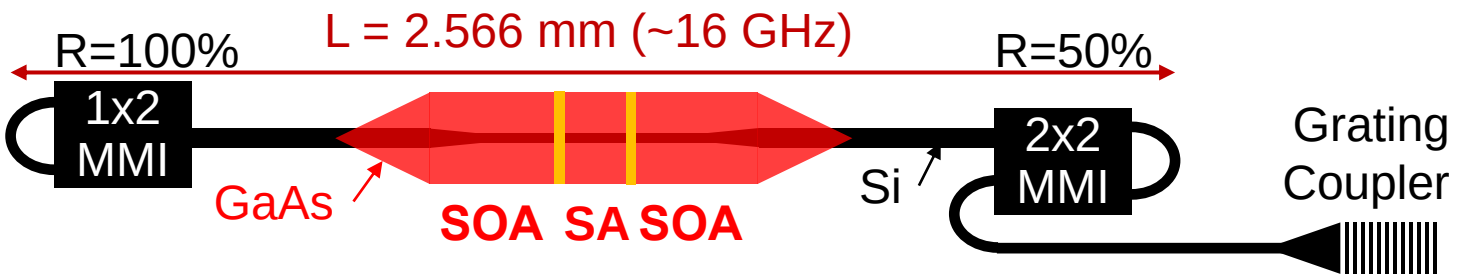
Comb laser

- Bond GaAs-based QD material to SOI
- Design layer thicknesses for efficient coupling between Si and III-V
- Adjust QD confinement through Si waveguide width

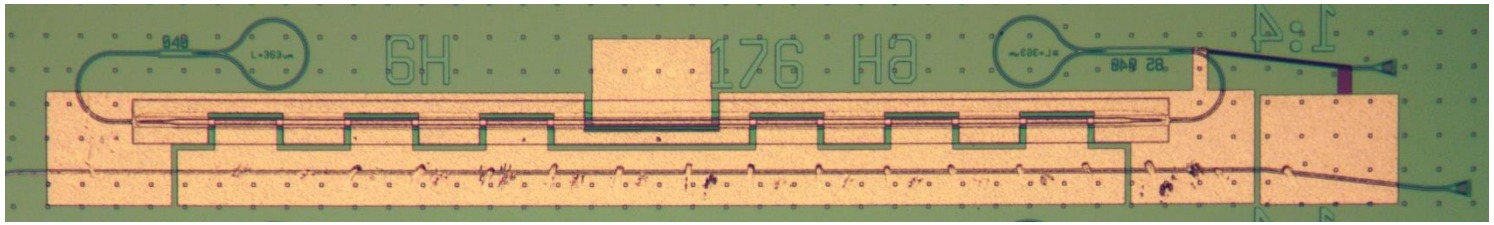




Comb laser design



L_{SOA} = 1200 µm
L_{SA} = 176 µm



- SOI: 400 nm Si (SOITEC)
- QD: 5 QD layers (QD Laser, Inc.)
- W_{mesa} = 6 µm
- W_{Si} = 475 nm
- Γ_{dot} ~4% ($\Gamma_{dot+barrier}$ ~35%)

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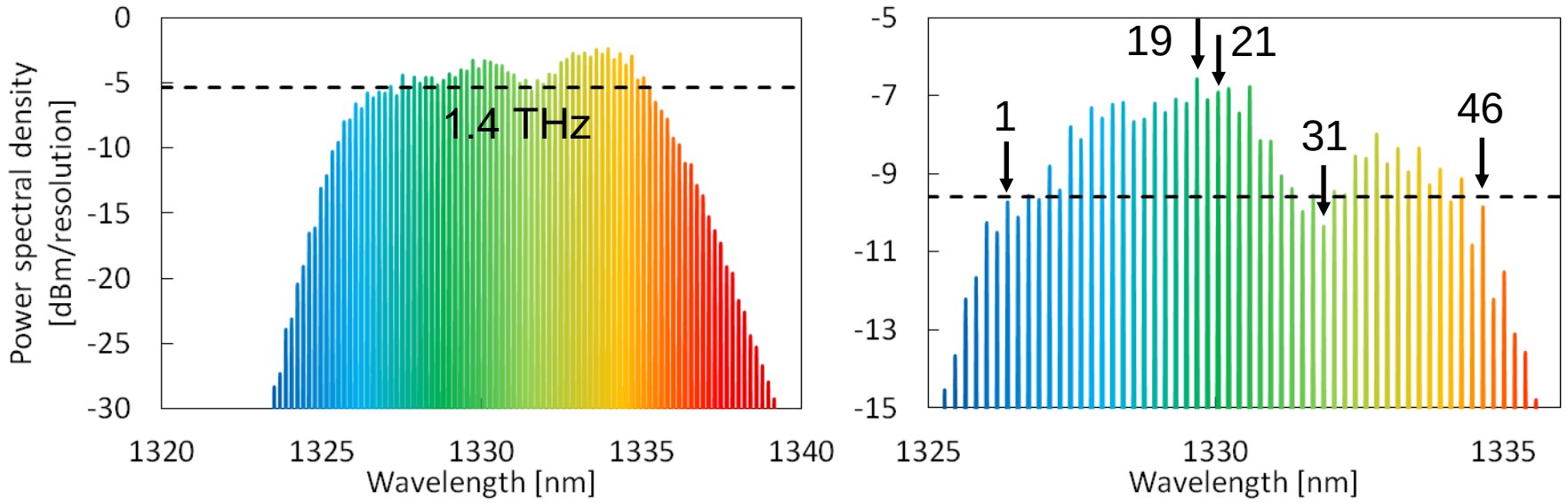
Comb laser data @ 50°C, continuous wave



– **Comb laser: 260 mA, 1.96 V → 509 mW**, SA = -6 V

– Channel spacing defined by lithography

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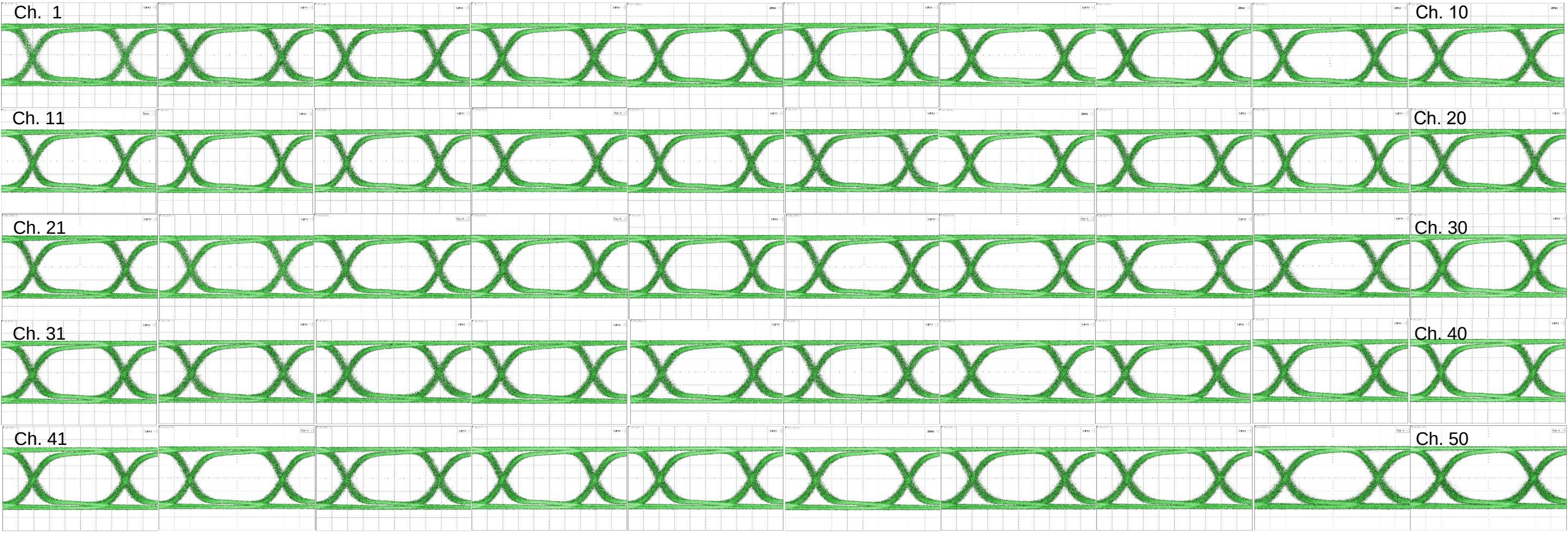
Comb laser data @ 50°C, continuous wave, !external! modulation



50 comb lines @ 10 Gb/s (setup limited) = 500 Gb/s with 509 mW laser power @ 50°C

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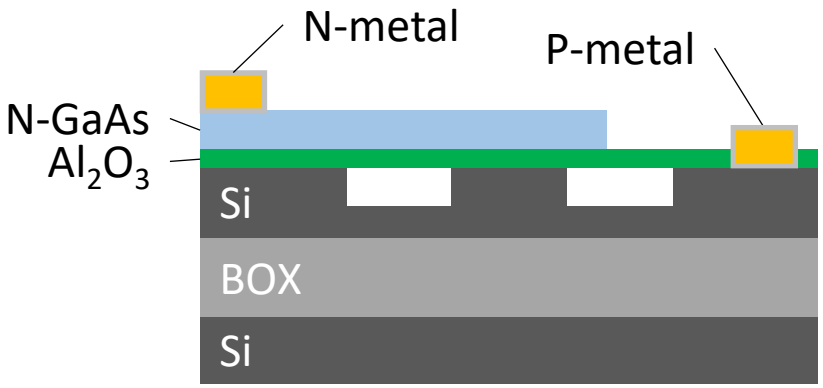
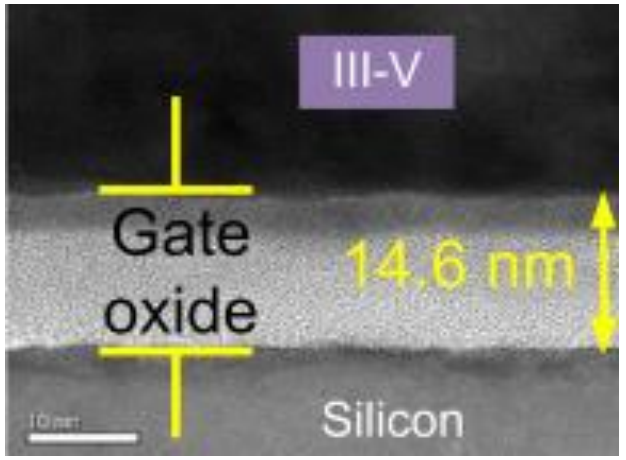
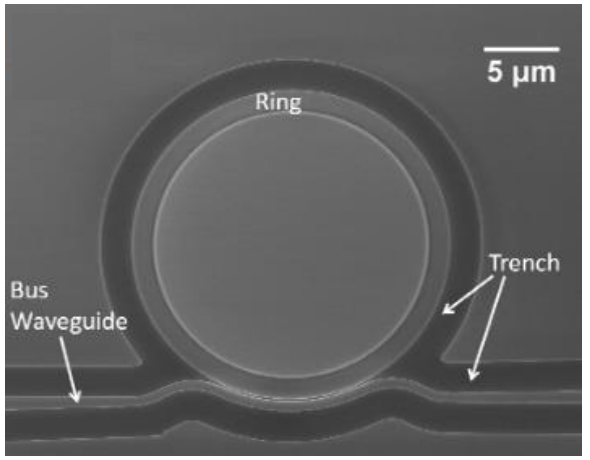
Wavelength tuning



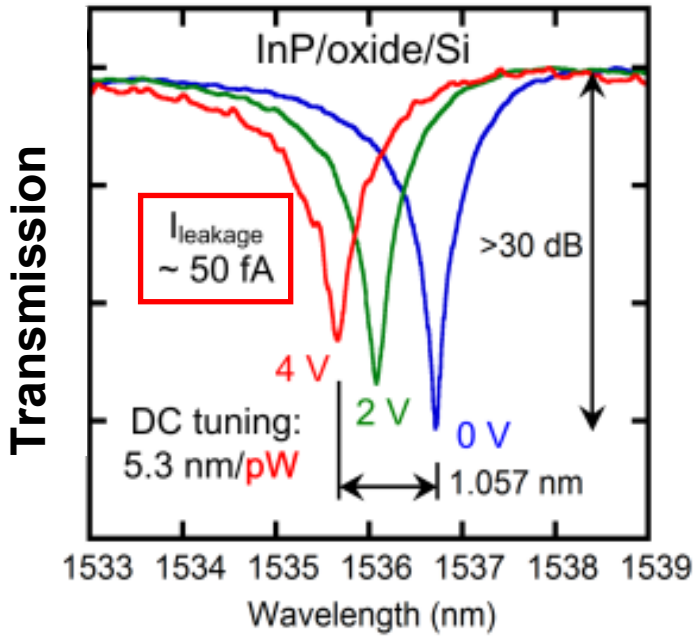




– Bonding oxide between III-V and Si forms inherent capacitor

– DC voltage → carrier accumulation → refractive index change → resonance shift

– No current flow → negligible power consumption



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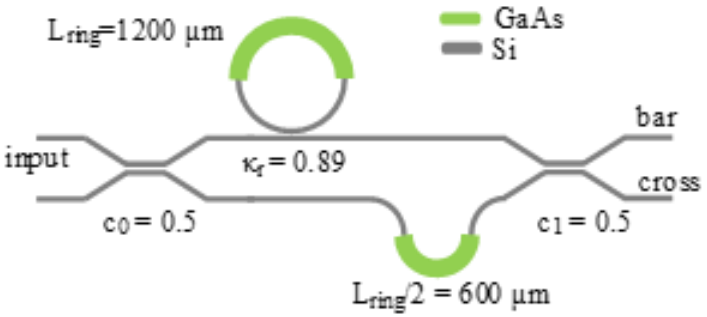
Deinterleavers

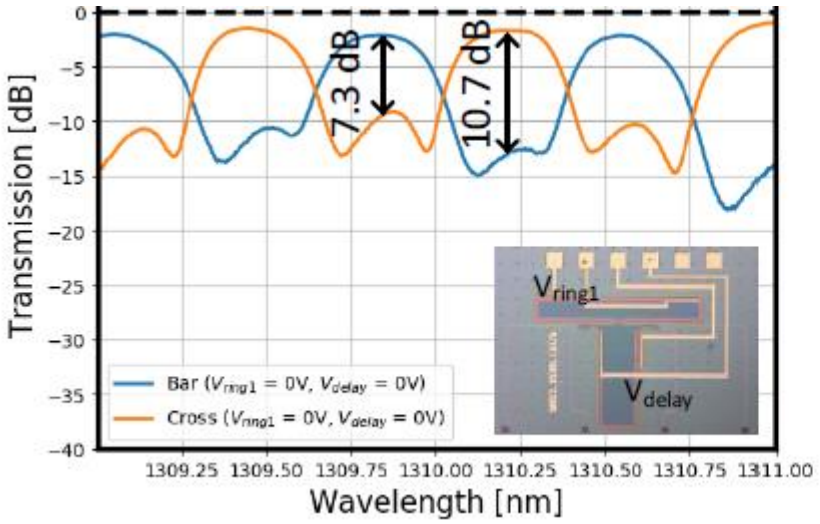
– Comb laser prefers small channel spacing (~30 GHz): wide comb

– Modulator prefers large channel spacing (~120 GHz): low insertion loss and crosstalk

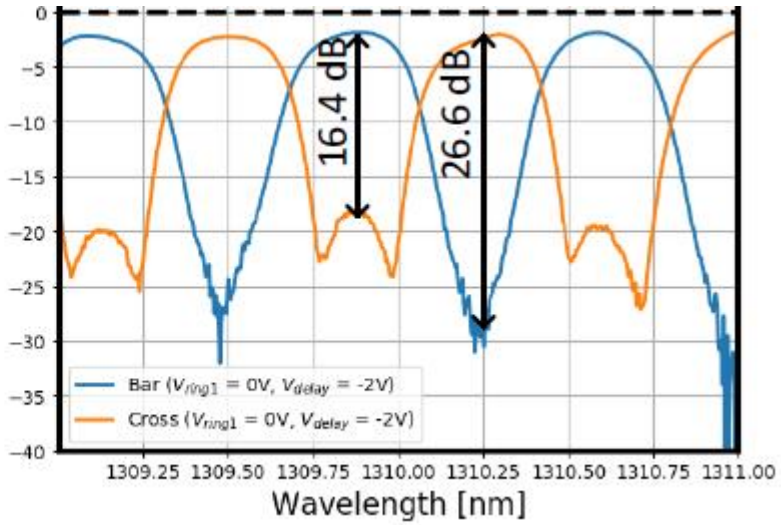
→ **Deinterleave 30 GHz comb into four spatial channels @ 120 GHz**



As fabricated

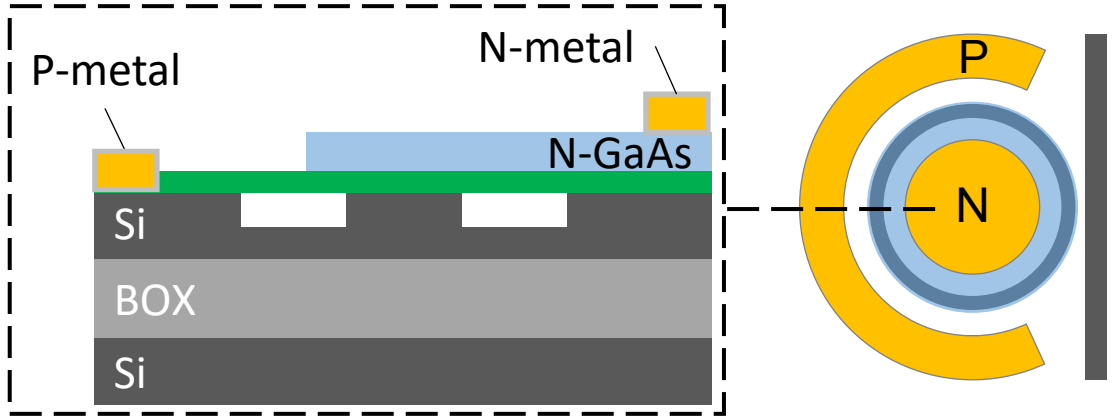


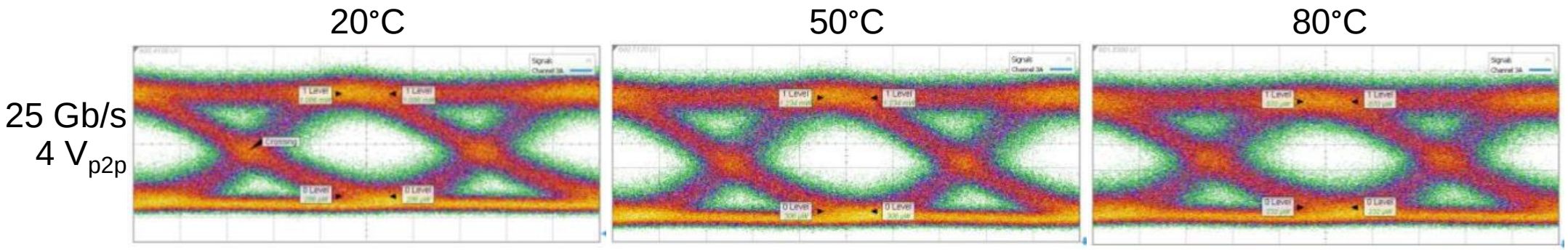
After MOS-based phase corrections



2 V, 5 nA → 10 nW

MOS Modulator





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Demonstrated so far

– All individual components (laser, deinterleaver, modulator, SiGe APD*) except for low loss grating couplers

*SiGe APDs demonstrated in external fab, not integrated with lasers

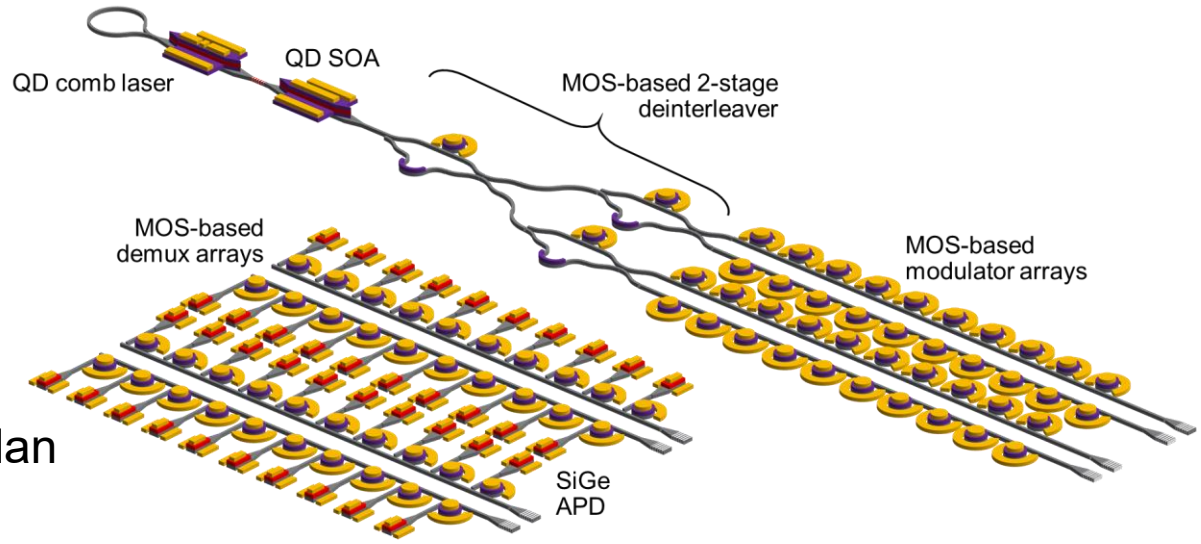
Remains to be done

– Low loss (≤ 3 dB) grating couplers

– Replicate SiGe APD performance in in-house fab

– Integrate everything on one chip

– Tie in design and characterization data to scale up plan



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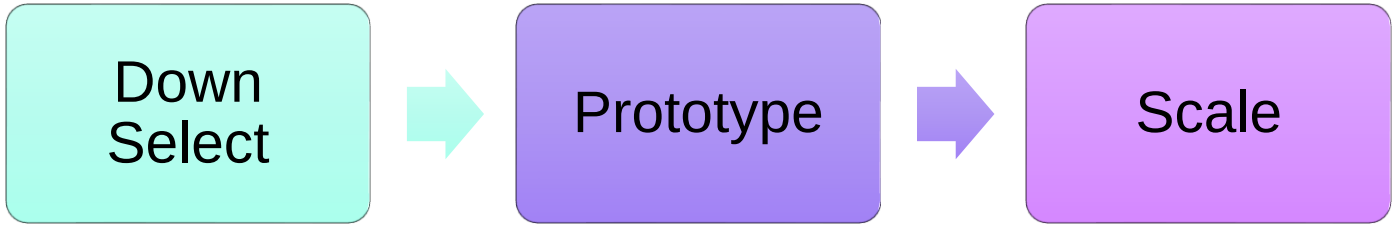
Path to Commercialization: Yield Management from Design Phase



- **Design phase (MPW/dedicated wafers) facilitate test of multiple design variants- evaluation metrics:**
  - Key performance targets met? e.g. Data rate, power consumption and BER
  - Robustness to process variation? i.e. performance of comb laser repeatably centered in process window
  - Designs which perform best to both above criterion chosen to Prototype

- **Prototype phase: special builds with detailed failure analysis- sample parts to System Level**

- **Select best performing design and material system to scale into full volume manufacturing**

Path to Commercialization: Primary Use Cases & Transition Plan

- **High Radix switching for High Performance Computing data fabric**
- **Low power AI Hardware accelerators**

Design Parameter	Current	Initial Scaling	Long Term Scaling
# Of channels	4 lanes	8 lanes	16 lanes
Bonded Area/ Wafer	20%	60%	80%
Material System	SOI/GaAs/SiGe	SOI/GaAs/SiGe	SOI/GaAs/InP/SiGe

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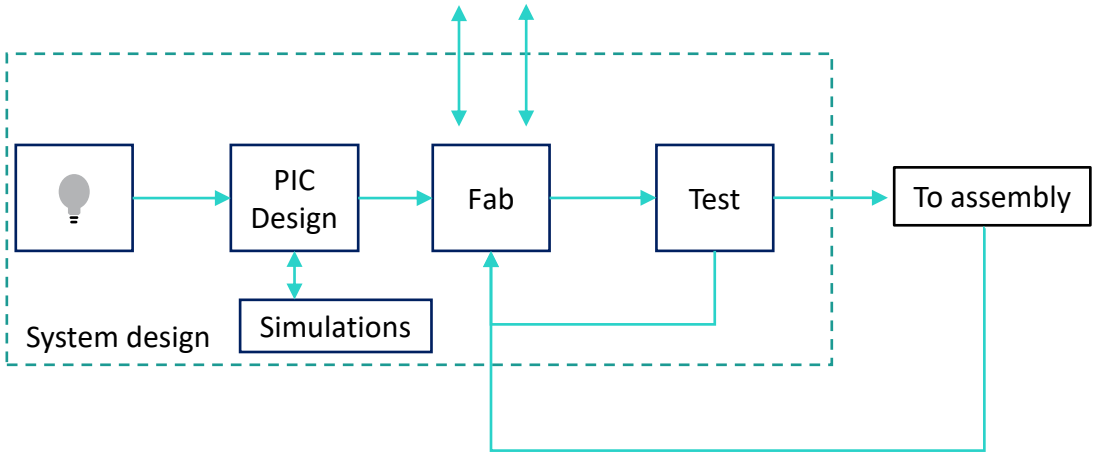
Path to Commercialization: Partners

Intermediate Read-out points
On Key Process steps



Use test and assembly data to tune Fab process to Optimal position

- **Ecosystem partners identified in US and Europe**
- **Engagement model and scaling objectives under discussion**
- **Model is to engage early in product lifecycle, design phase through packaging and test with close yield monitoring**
- **Transparent data flow with traceability end to end key to successful scaling**

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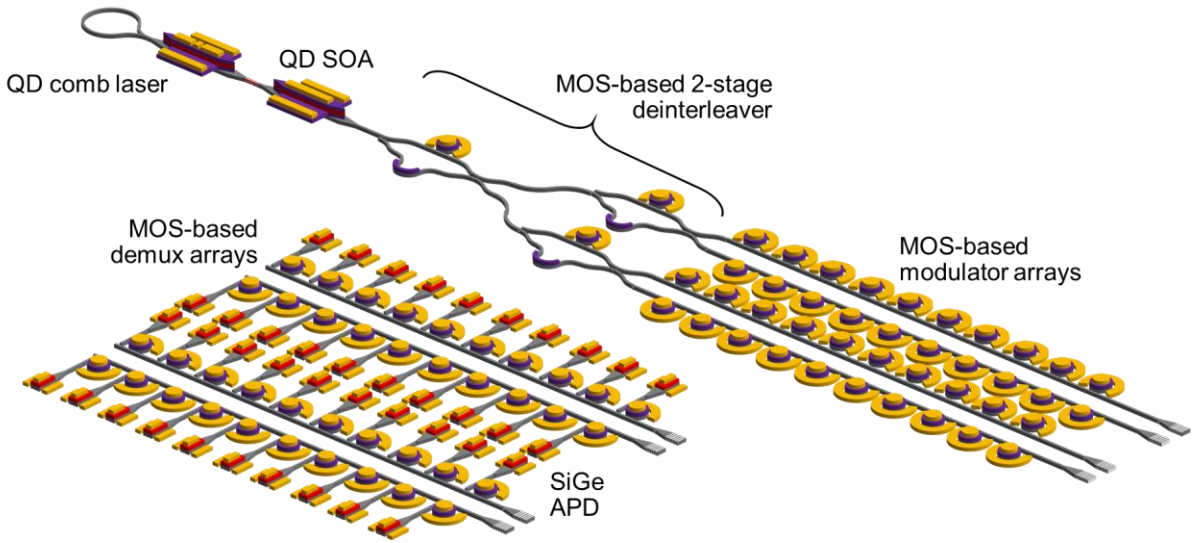
Summary: Technology and Path to Scale

Concept → Devices → Subsystem → System → Revenue



- Deploy technology into energy efficient High Performance Compute and AI HW accelerators at scale

- Following individual components to demonstrate >1 Tb/s, <1.5 pJ/b* link have been fabricated and characterized: Laser, deinterleaver, modulator and SiGe APD*

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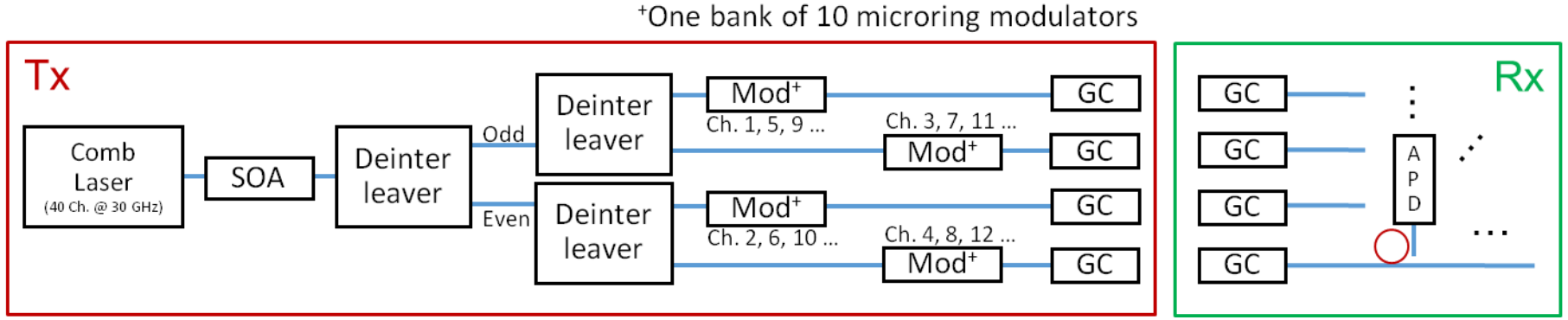
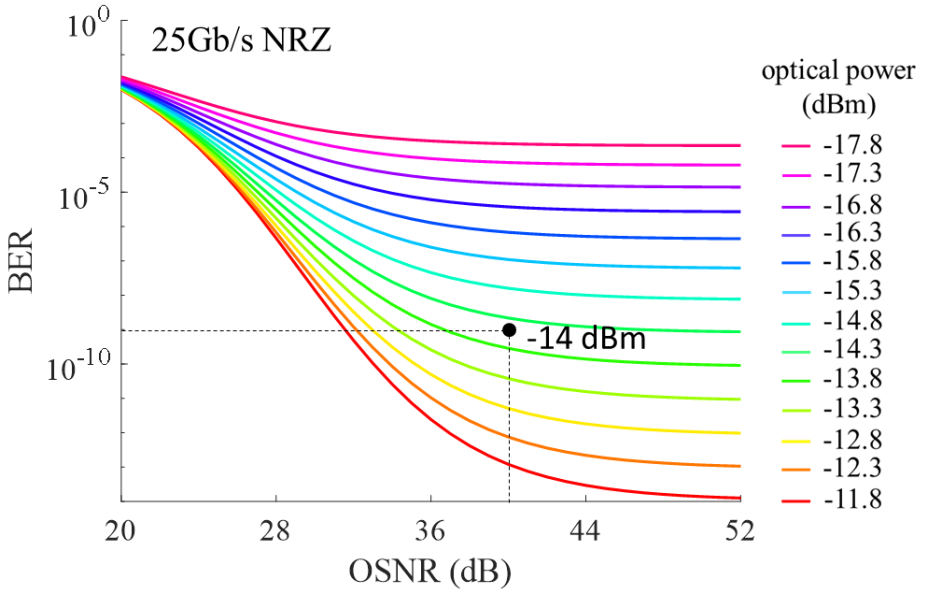
Backup

Transceiver chip energy efficiency goals





50°C				Single ch.	**N= 40**
Comb laser			**-12.2 dBm/channel**		500.0 mW
Amplifier	15	1	15.0 dB		300.0 mW
Deinterleaver	0.5	2	1.0 dB		
Modulator	0.3	1	0.3 dB	0.58	23.2 mW
GC loss	3	1	3.0 dB		
Passive WG loss	5	1	5.0 dB		
Fiber (10 km)	4	1	4.0 dB		
GC loss	3	1	3.0 dB		
Demux	0.5	1	0.5 dB		
PD Sens			**-14.0 dBm**	1	40.0 mW
					863.2 mW
				25	1000 Gb/s
					0.86 pJ/bit

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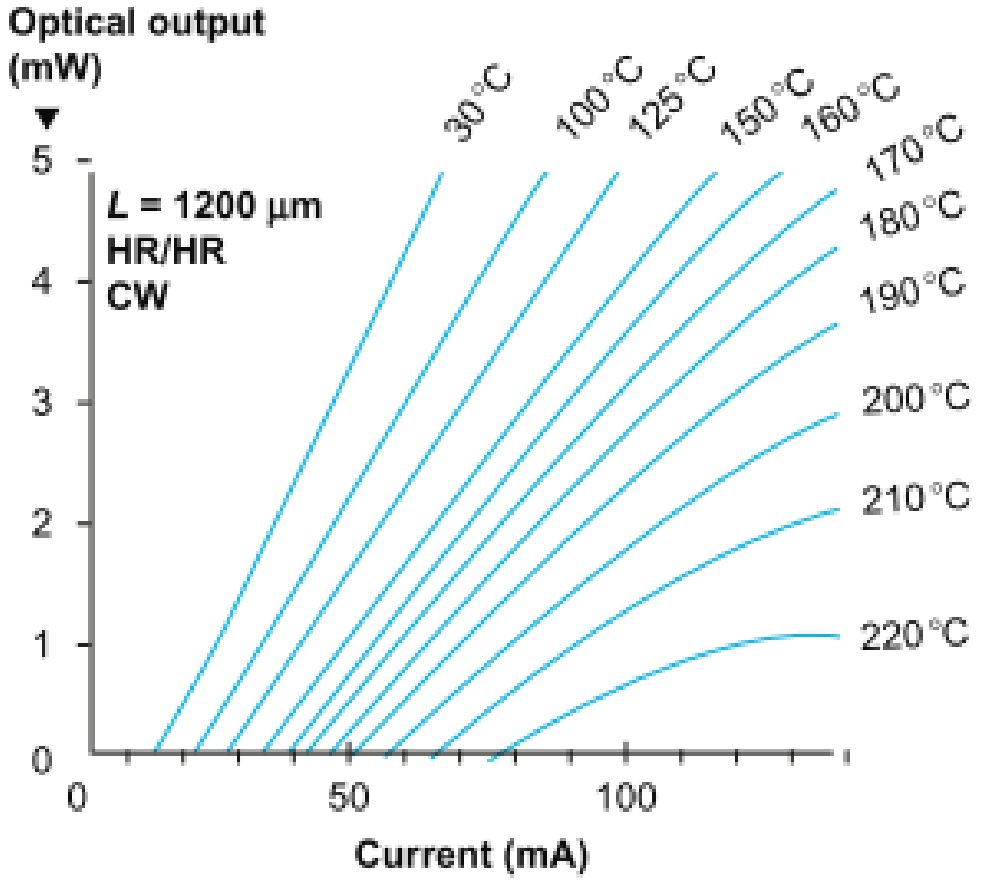
Comb laser requirements

- Wide gain bandwidth
- Operation at high temperature
- Low amplitude noise in ***!EACH!*** comb line

  → **Quantum dot lasers …**
- Integration with high quality passives
  - Gratings, splitters, rings, …
- High yield, volume foundry
- On 300 mm wafers

  → **… on silicon**

Don't just use Si as a carrier. Take advantage of its excellent passive devices as well!



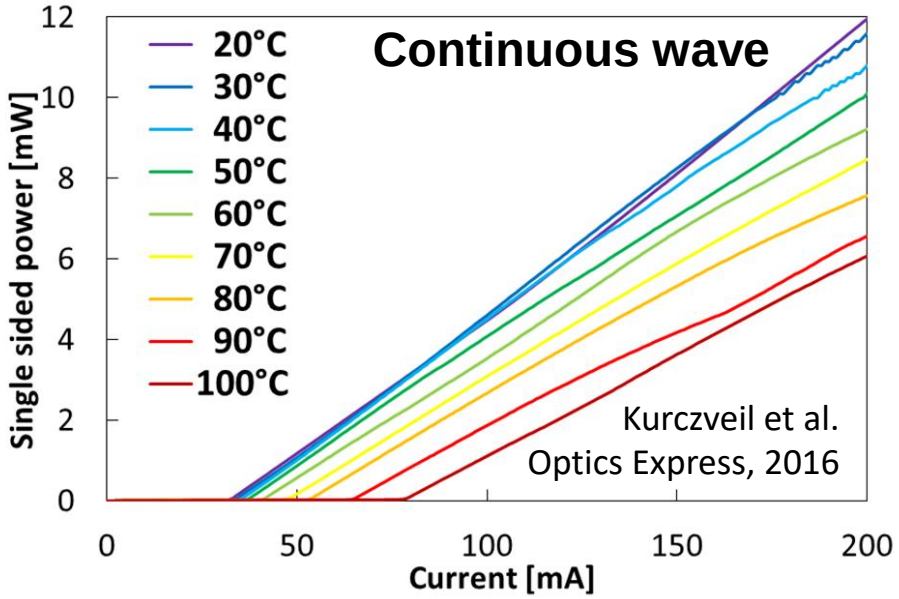
QD Laser Inc., 2011

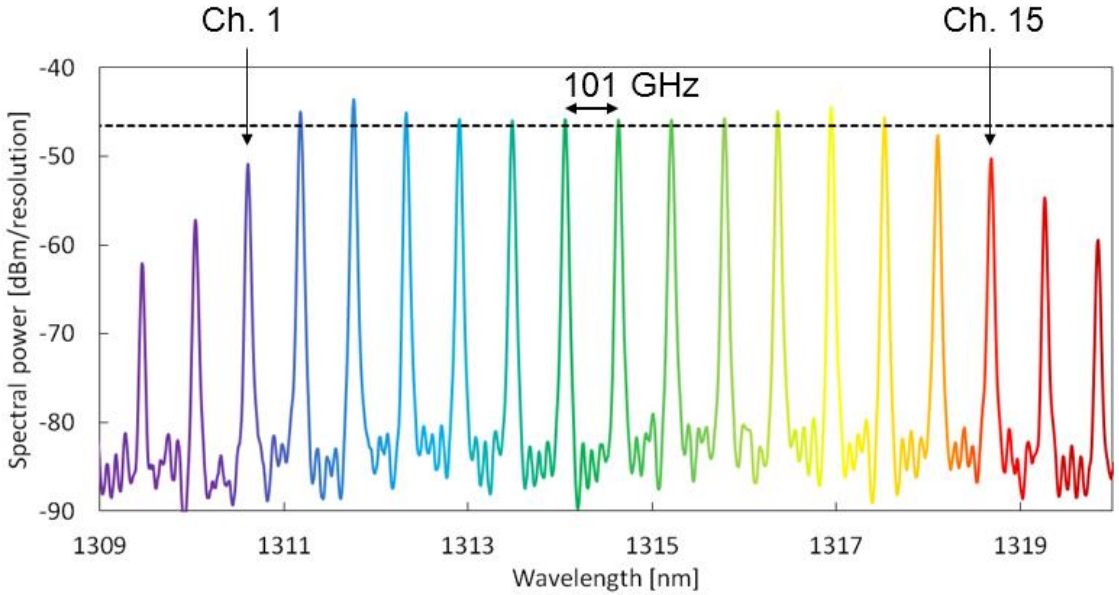
Previous results

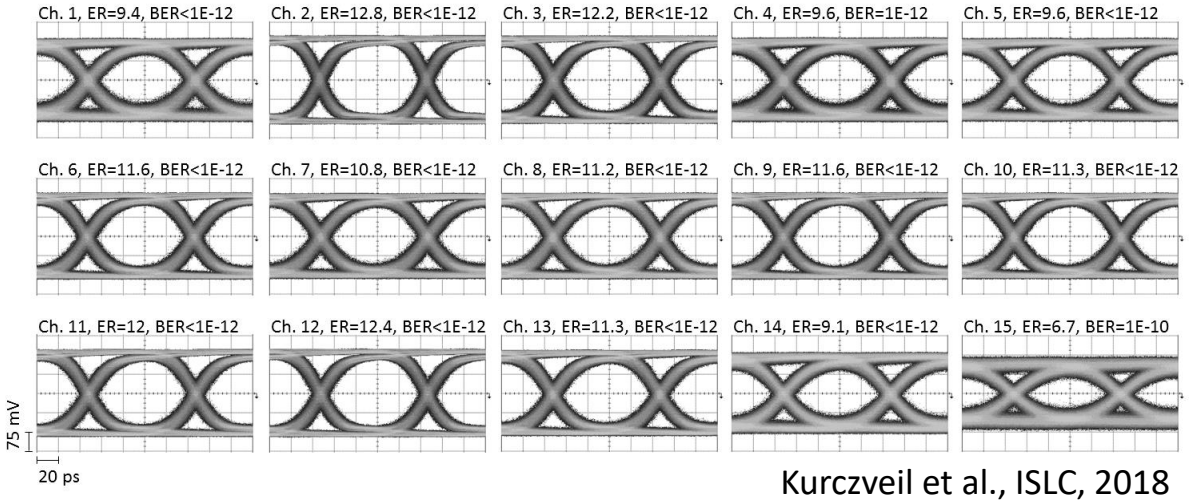
–100°C operation (CW)

–3 dB bandwidth: ~6 nm, 12 channels

–FEC-free BER ≤ 10^{-12} in 14 channels (10 Gb/s, NRZ) @ 20°C







Kurczveil et al., ISLC, 2018

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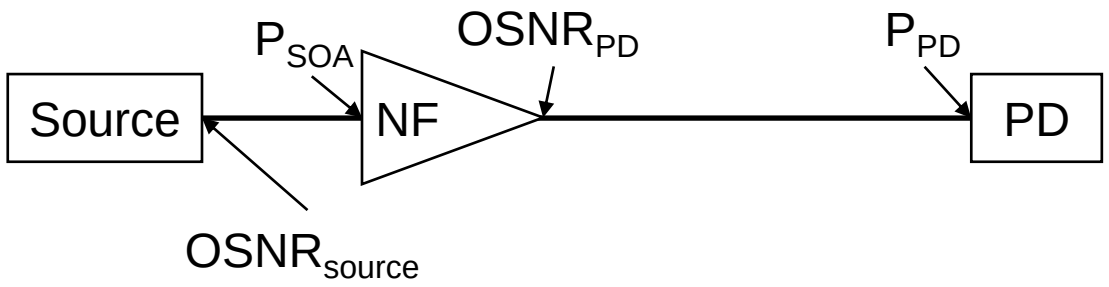
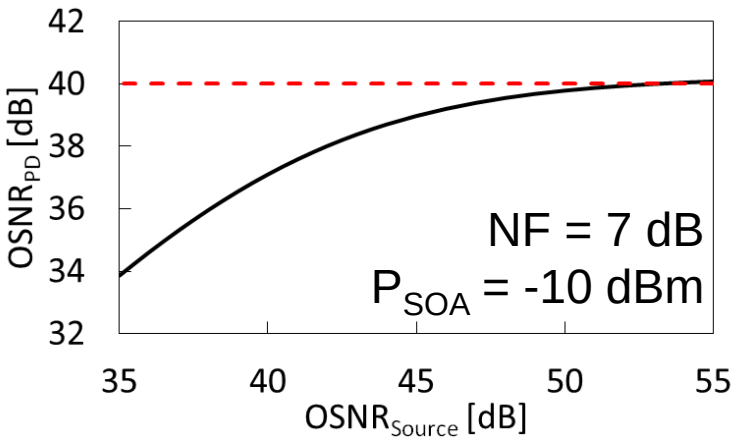
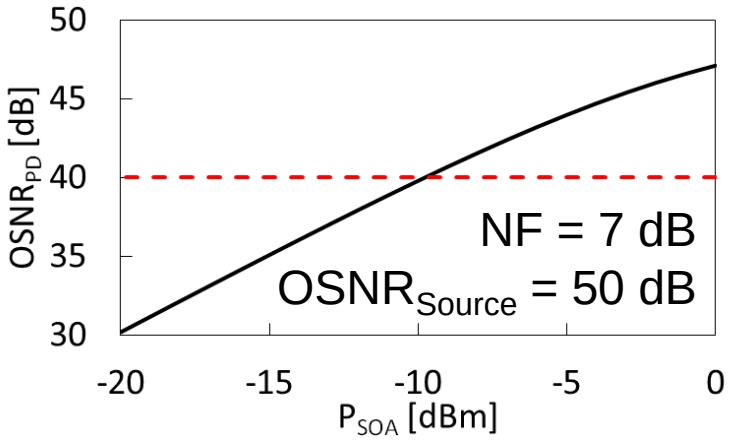
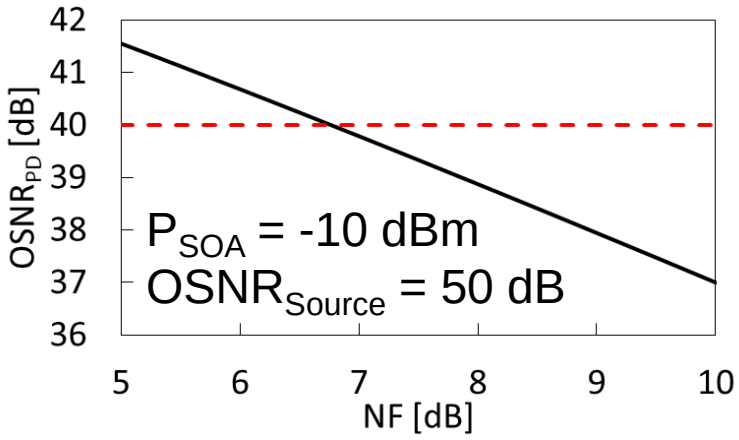
OSNR



$$\frac{1}{OSNR_{PD}} = \frac{1}{OSNR_{Source}} + \frac{NF \cdot E_{photon} \cdot \Delta f}{P_{SOA}}$$







↑ OSNR by:

- ↑ P_{SOA} → Place SOA right after comb laser
- ↓ NF of SOA

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