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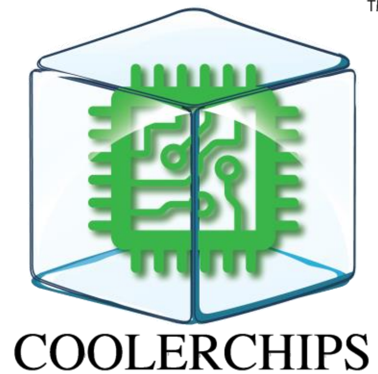
CHANGING WHAT'S POSSIBLE

Sub-One System
Dr. Ludwig Haber, JetCool Technologies



Project Vision

- Eliminate Facility Air Cooling at the Server Level
- Use Micro-convective cooling to operate silicon at highest electrical efficiency
- Reduce server fan power consumption by eliminating exchange with data center air

COOLERCHIPS Kickoff Meeting
October 18 & 19, 2023

Total Project Cost:	$1.26M
Length	24 mo.

Brief COOLERCHIPS Project Overview

Fed. funding:	$1.26M
Length	24 mo.

Team member	Location	Role in project, core competencies
JetCool Technologies Inc.	Littleton MA	Prime, micro-convective cooling, micro-channel Hx's, product development
Sandia – Manzano Data Center	Albuquerque NM	Technology verification site

Sub-One System for Silicon Efficiency and Elimination of Air Cooling to Server

Combine micro-convective heat transfer at the CPU / GPU with innovative micro-channel radiators in-server to eliminate facility supplied air cooling in the server.

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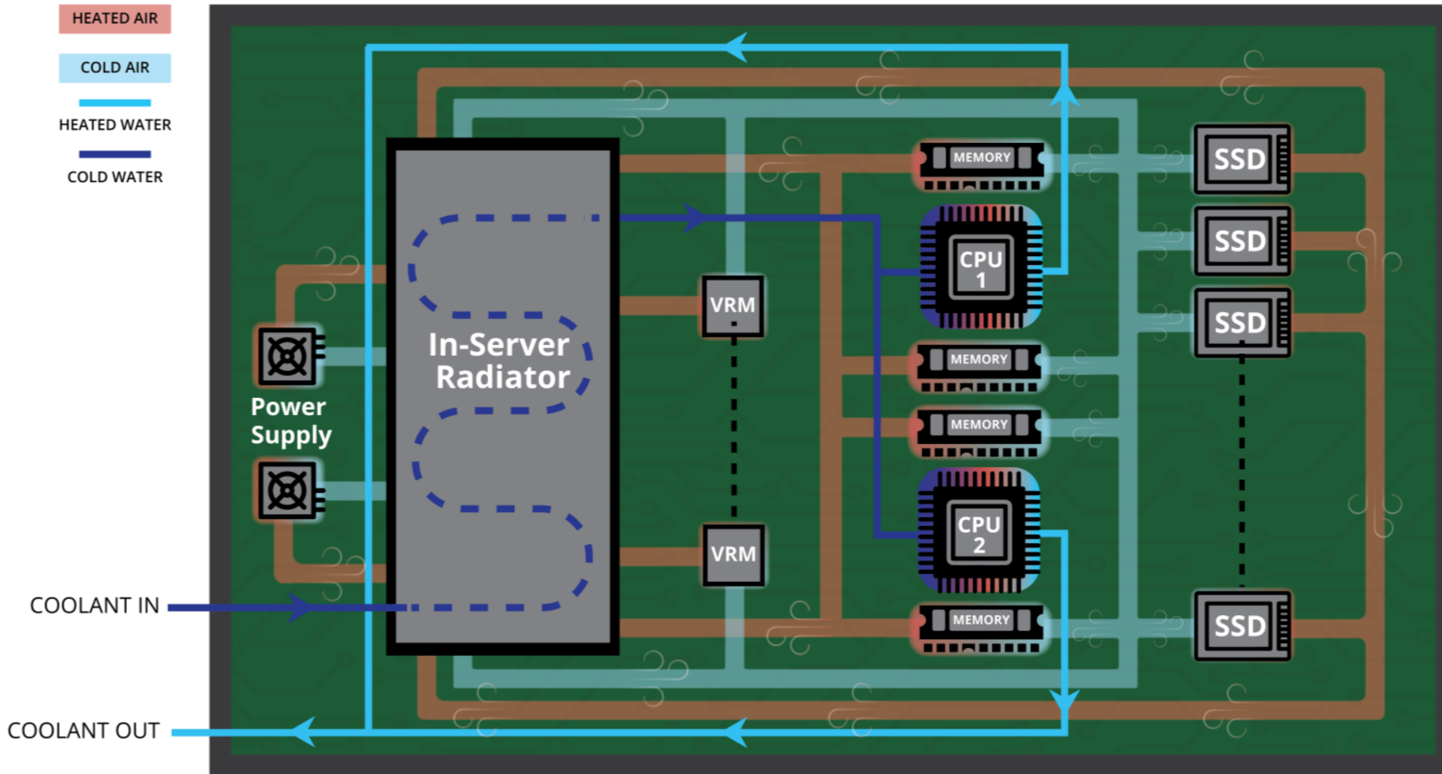
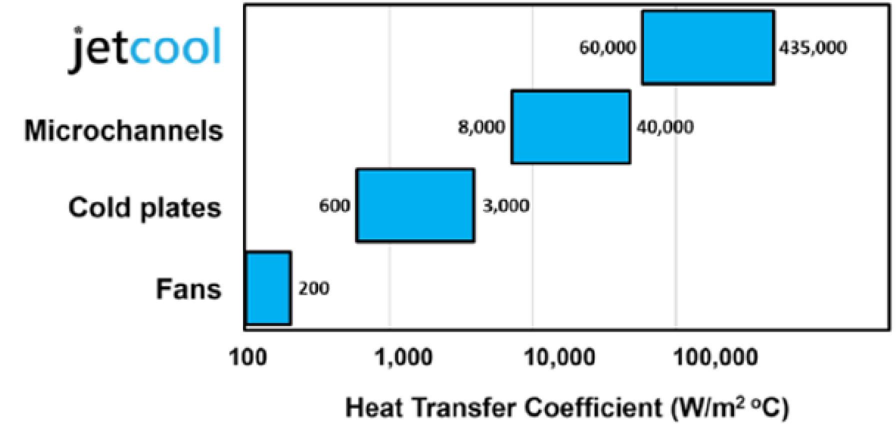
Concept Detail



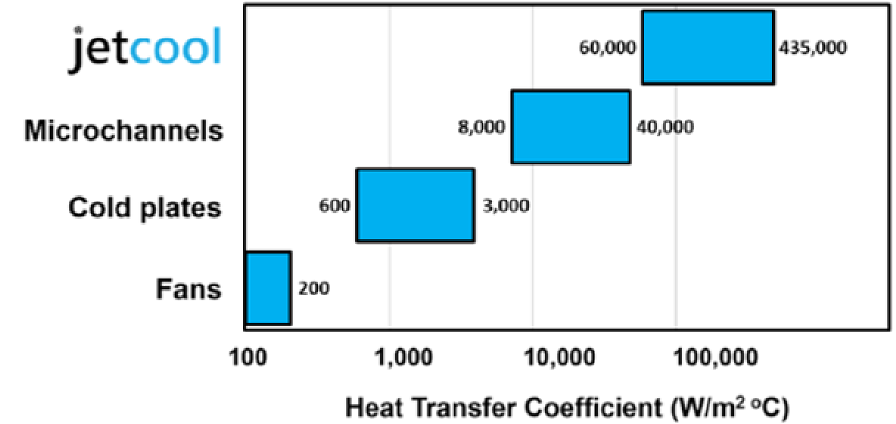


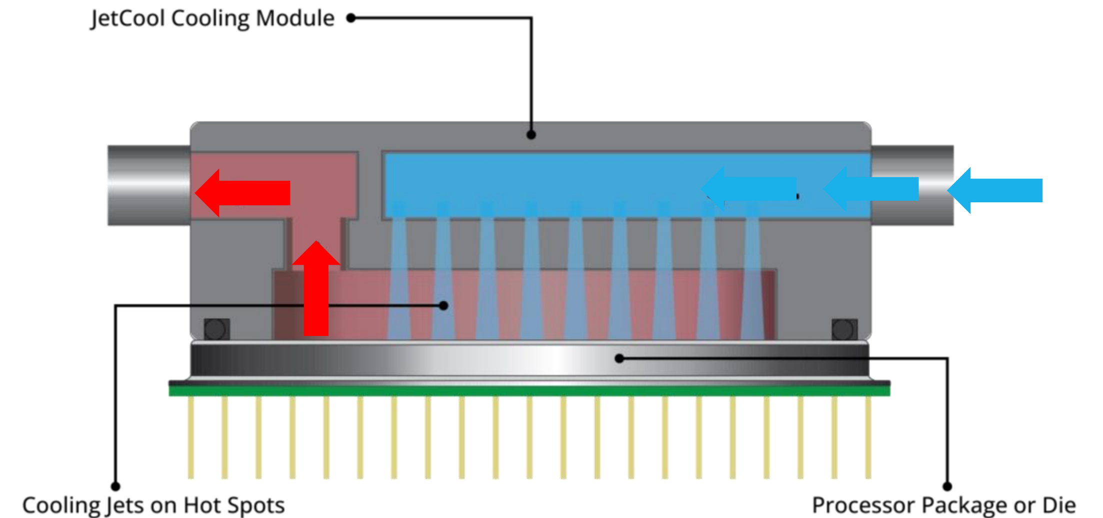
- Micro-convective cooling direct-to-lid
- Compact micro-channel radiator for in-server cooling

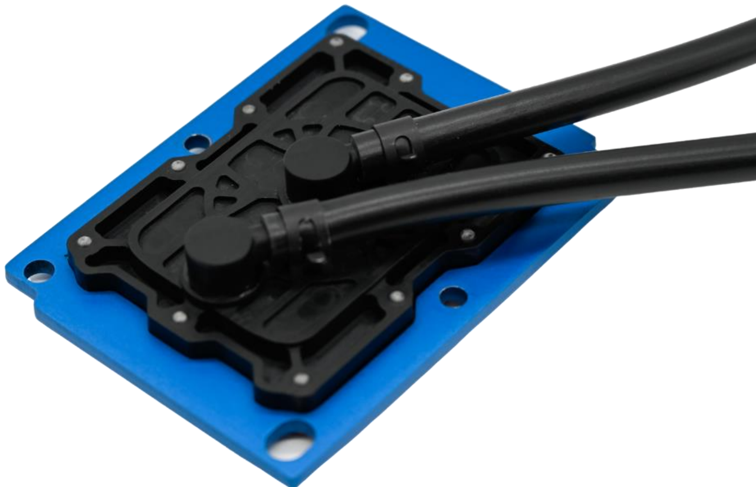
FOA Metrics	Units
Resistance Target (case to fluid)	0.009 K/W
Cooling Power % of IT_power	<3 %
System availability	99 %
Chipset	3rd / 4th Generation Intel Xeon 3rd / 4th AMD EPYC
Chip Power	200-400W
Power per server	Current validation platform is 1/3 U dual CPU slices. 6 CPU's per U.
Validation power mid project	12 kW

Micro-convective Cooling

- Target hot spots
  - Concentrate cooling at highest heat flux
- Performance improves for warmer coolants
  - Reynolds number dependence
- Lower spreading is preferable
  - Get to source and minimize flow
  - Maximize heat flux







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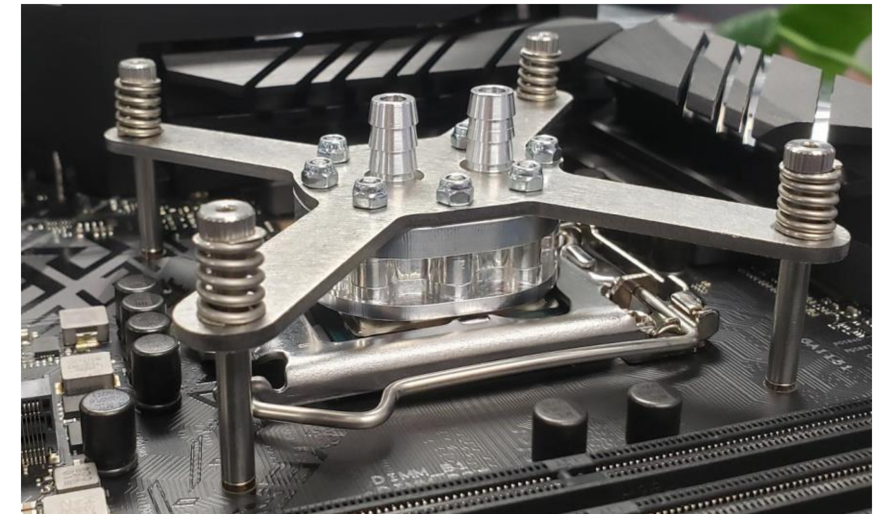
Task Outline & Technical Objectives

- *Phase 1 (6 mo):*
  - *Develop micro-convective cooling architecture analytically*
    - *Validate performance targets in heat transfer and fluid power*
  - *Develop micro-channel radiator architecture analytically*
    - *Validate air distribution and component cooling performance*
- *Phase 2 (18 mo):*
  - *Experimental verification of Sub-One system at 12 mo*
  - *Reliability testing and modeling at 18 mo*
  - *12kW deployment prior to completion*



Intel i7 direct to lid cooling prototype

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Challenges and Risks

- *Fundamental technology has been proven many times over*
  - *Constraints provide most of risk*
- *Reliability is the key to commercial success and must be addressed early and often*

Likelihood	Insignificant	Minor	Moderate	Major	Catastrophic
Almost Certain					
Likely		6	2	3	
Moderate			4	5	7
Unlikely				1	
Rare					

Consequences

Risk Status

Risk	#
Case-to-fluid thermal resistance	1
Lack of accurate heat flux maps	2
Exceeding fluid power target	3
Chip temperature above 60 °C	4
Excessively large radiator required	5
Pressure requirement for direct system tie-in	6
System reliability	7

Technology-to-Market Approach

- *JetCool is already entering the market with competitive products:*
  - *Smart Plate System: Bridge to liquid cooling*
  - *Smart Plate: Aggressive performance cold plates for the newest processors*
- *Key to* ***Sub-One*** *Commercial Success:*
  - *Leverage existing partnerships among OEM, end-user, and chip manufacturers*
- ***Sub-One*** *Markets:*
  - *Near term: Edge computing (Sub-One offers easier implementation with no server HVAC impacts)*
  - *Long term: HPC data centers with applications in AI, HFT*

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Needs and Potential Partnerships

- *JetCool has developed product specific reliability models but needs to integrate these in data center level reliability modeling. Looking for partners in the COOLERCHIPS community !!*
- *Current technology validation cluster is 2nd Generation Xeon*
  - *Meets power density requirements*
  - *Sandia / Manzano is great to work with*
  - *Possible desired improvements in technology validation platform:*
    - *TDP is relatively low at 200W / processor*
    - *Does not contain challenge of addressing storage cooling*
    - *Looking for alternative cluster conversions (and optional revert-back)*
- *Cooling infrastructure:*
  - *Challenge question: Can the rack-level or row-level CDU be integrated with primary loop ?*

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