



New Topologies and Control Methods for Extreme Power Density Inverters: A Google/IEEE Little Box Challenge Case Study

Robert Pilawa-Podgurski

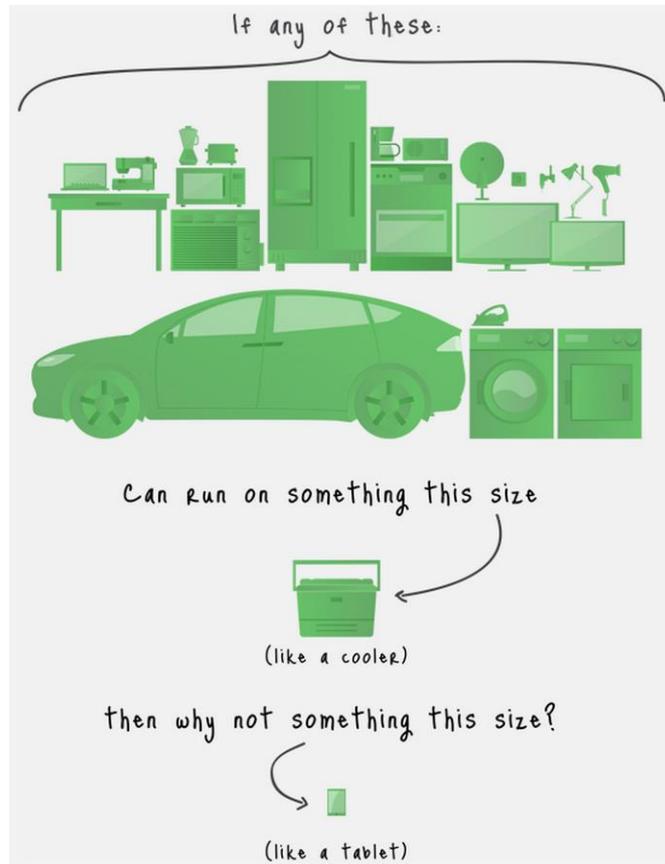
Assistant Professor

Department of Electrical and Computer Engineering

University of Illinois Urbana-Champaign

<http://pilawa.ece.illinois.edu>

ARPA-E CIRCUITS Workshop, September 13th, 2016



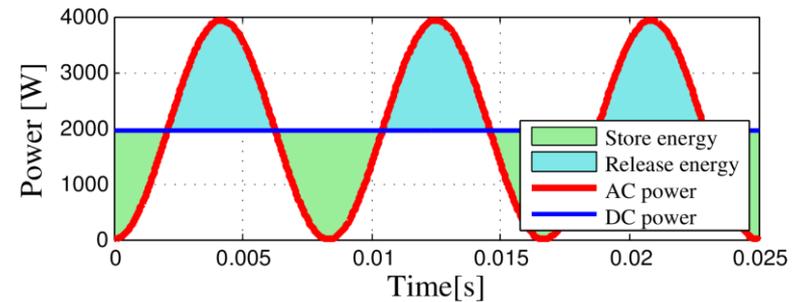
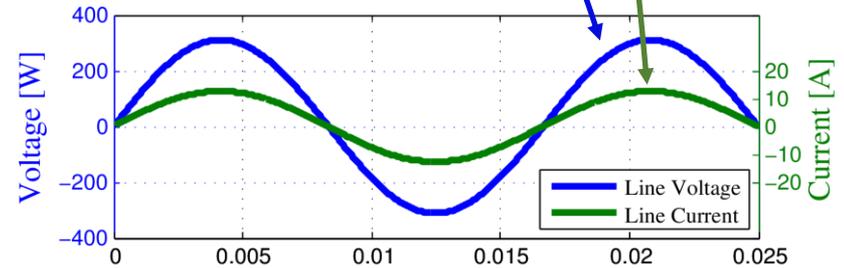
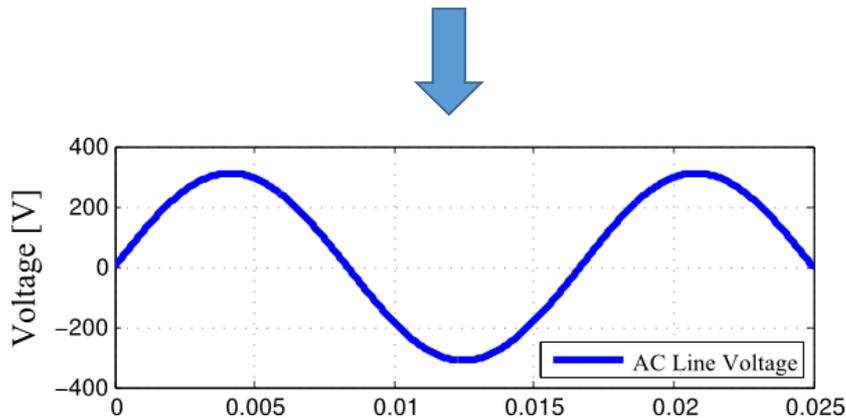
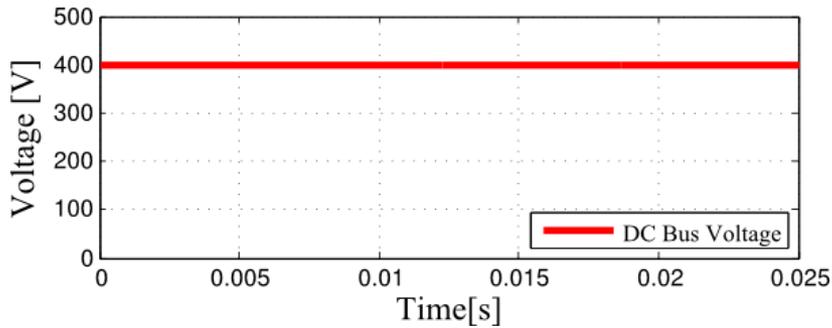
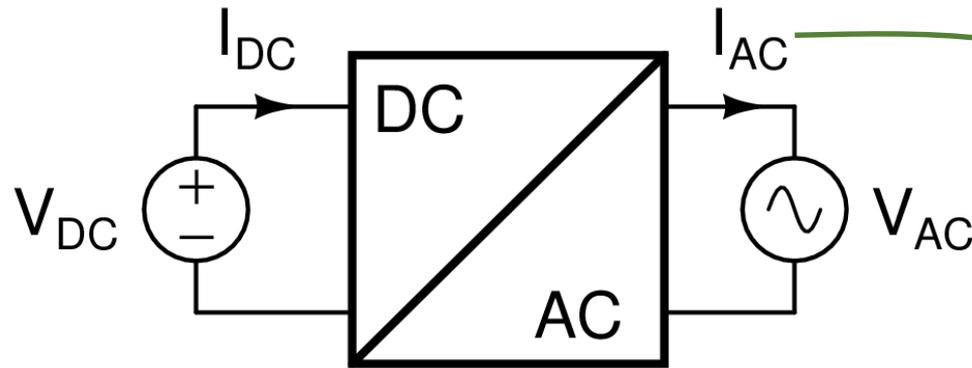
LITTLE BOX CHALLENGE

Google |  IEEE

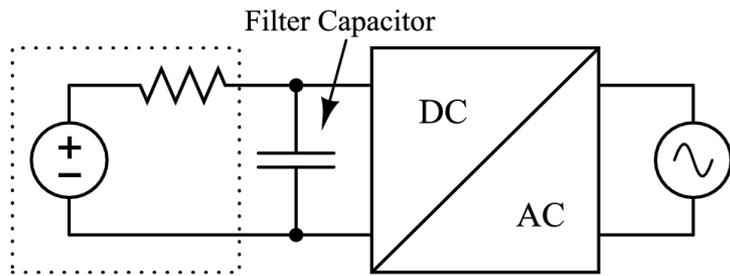
- 2 kW, single-phase 240 V, 60 Hz AC
- Example usage: solar inverter, electric car charger, grid storage integration
- Current state-of-the-art: 95% efficiency, 400 in³.
- Target goal: >95% efficiency, 10x smaller (40 in³), must run for 100 hours
- \$1M prize to winning entry

Our only chance was to do something no one had ever done before

Key Technical Challenges

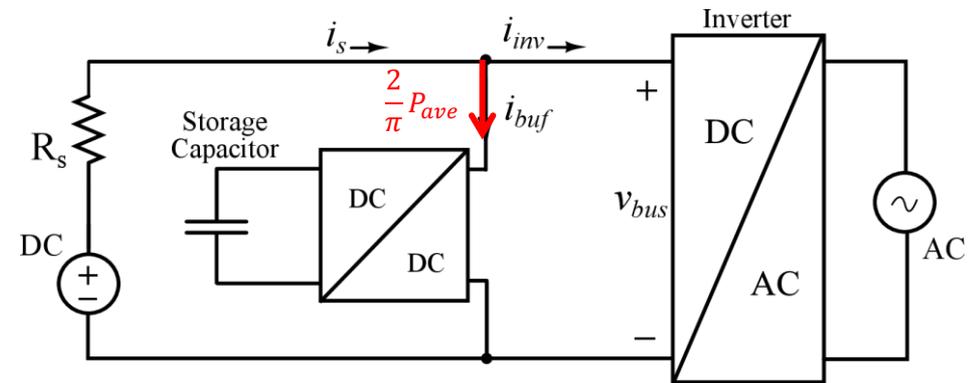


$$E_{store} = \frac{P_{dc}}{2\pi f_{line}}$$



Passive filtering

- No power processing
- Poor energy utilization of capacitor
- Large volume required for capacitor

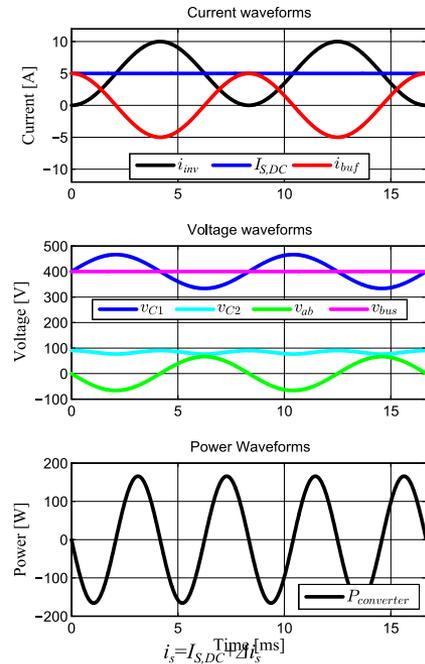
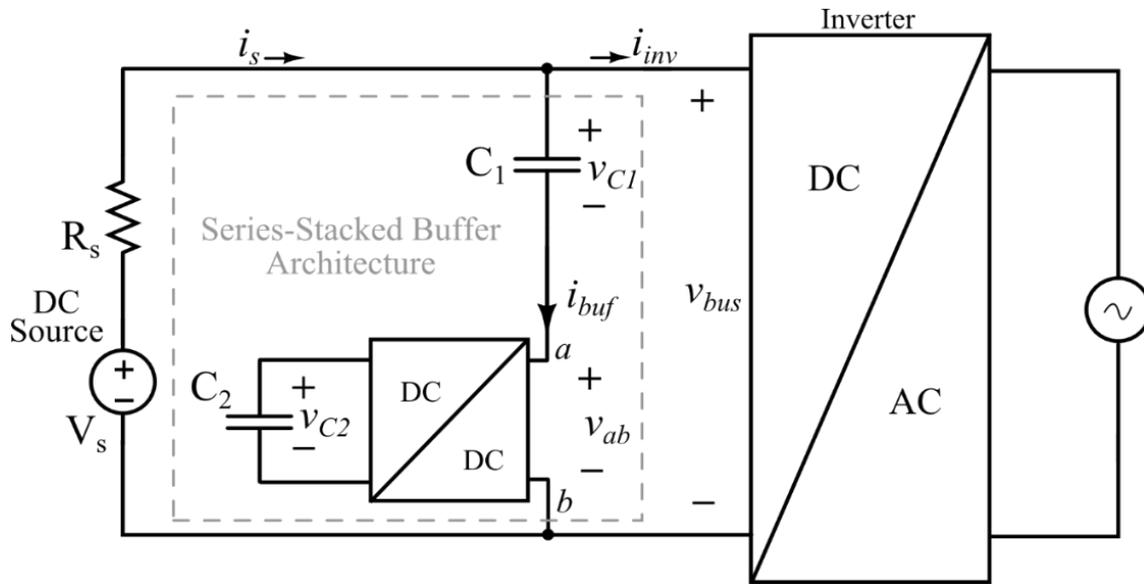


Full ripple port converter

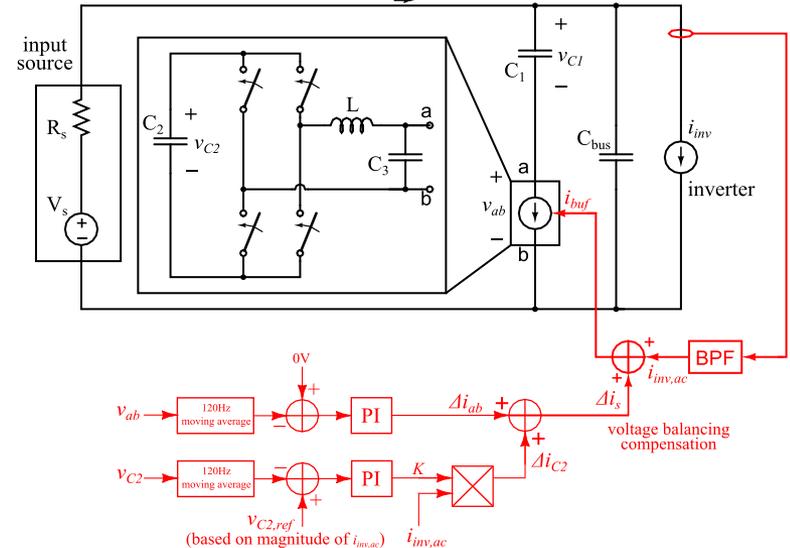
- High utilization of capacitor energy -> small capacitor size
- Increased power processing (and losses)
- Large volume required for ripple port converter



Series-Stacked Buffer Converter



- A series-connected buffer converter
 - Reduced voltage stress (C_1 blocks majority of voltage)
 - Enable low voltage transistors -> Buffer converter size reduction
 - Partial power processing (extreme efficiencies possible)
 - Low power rating of buffer converter
 - Size reduction



Hardware Prototype – Energy Density



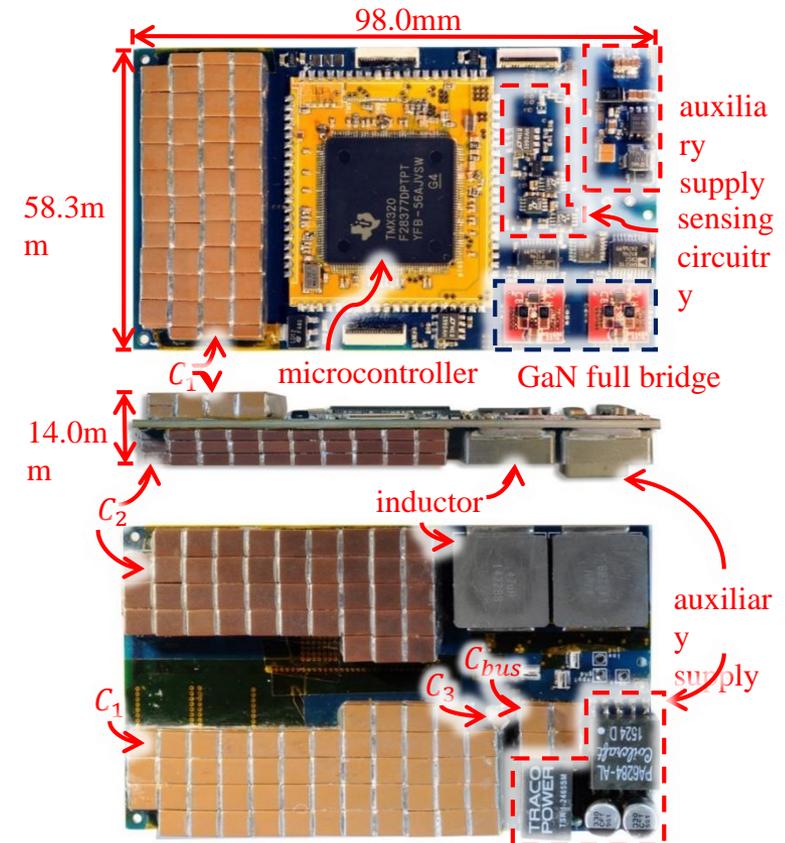
Design requirement:

- 2 kVA (PF = 0.7~1)
- 400 V ~ 450V bus voltage,
- 10 A peak to peak current

Way of measurement	Volume	Power density
Rectangular box	4.88 inch ³	410 W/inch ³
passive component	2.01 inch ³	995 W/inch ³

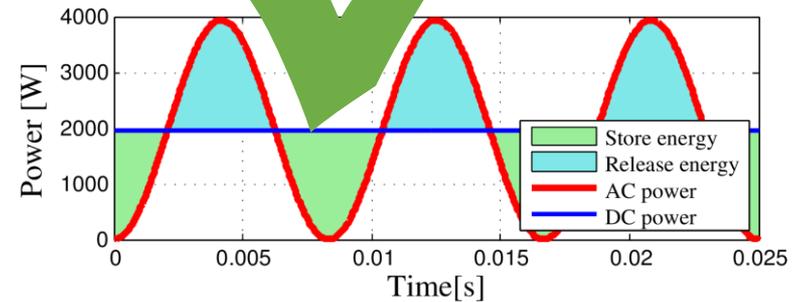
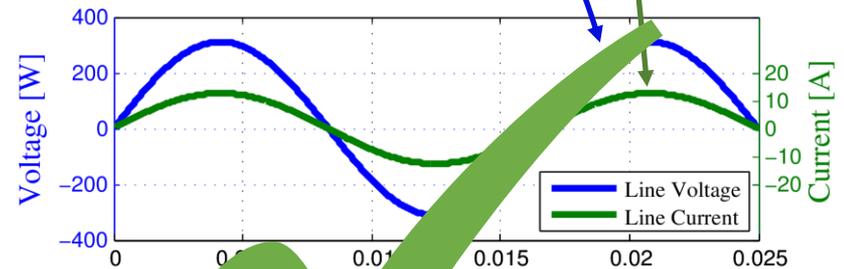
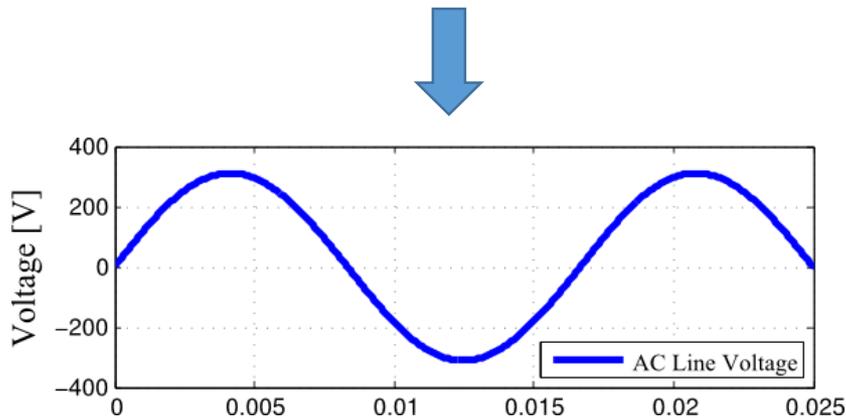
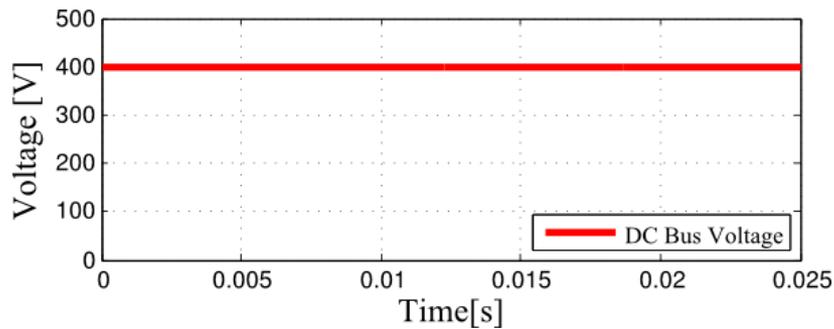
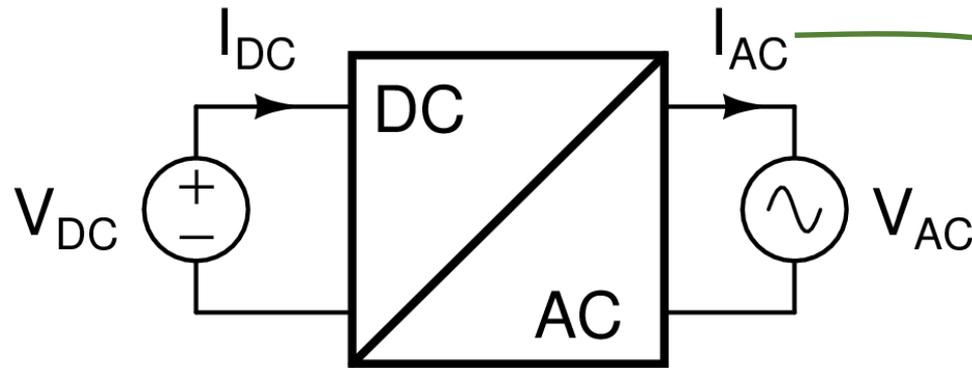
Key enablers:

- Reduced switch voltage
 - Stacked topology
- Partial power processing
- Sophisticated digital control



> 99% efficiency
across load range

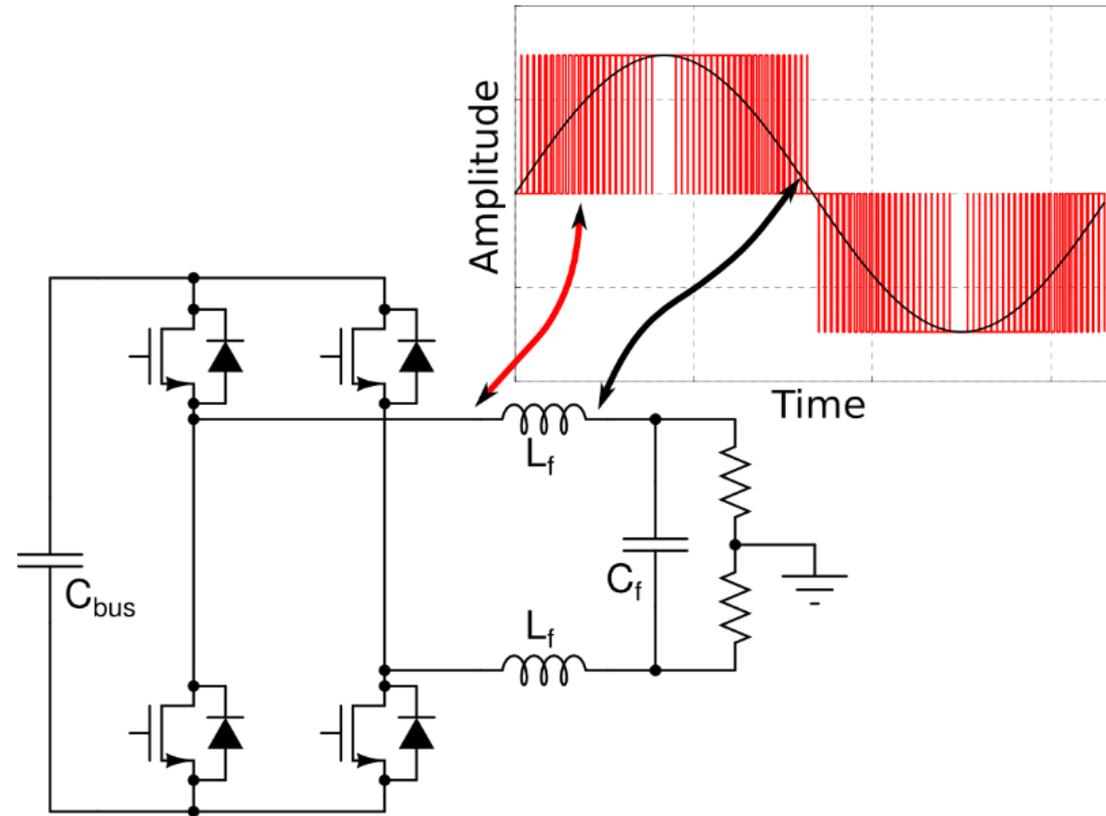
Key Technical Challenges



$$E_{store} = \frac{P_{dc}}{2\pi f_{line}}$$



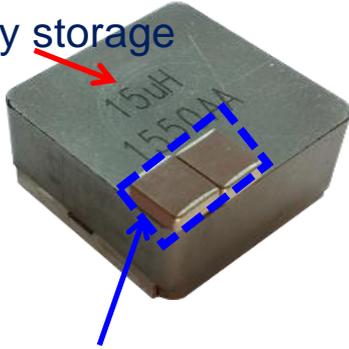
- Conventional Inverter
 - H-bridge topology
 - Maybe interleaved
 - 650 V GaN transistors
 - High switch stress
 - High dv/dt
 - Large inductor
 - Localized hot spots
 - Significant EMI!



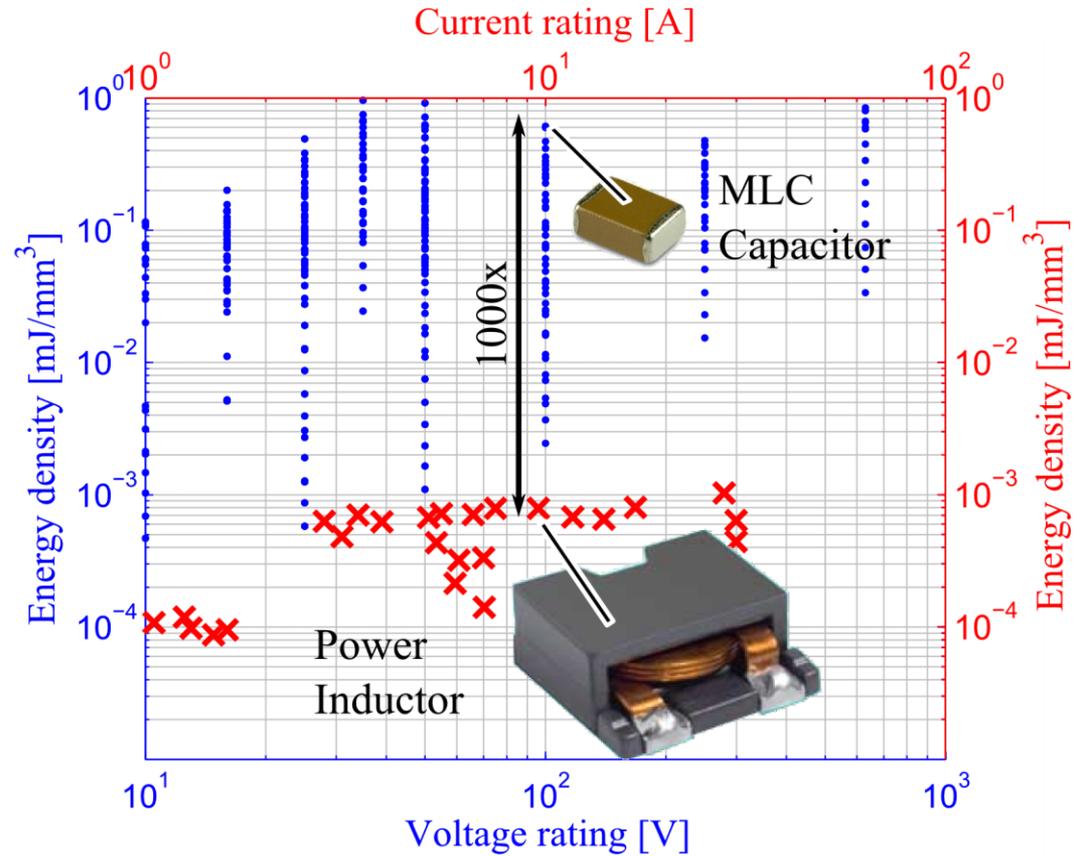
Choice of Passive Components



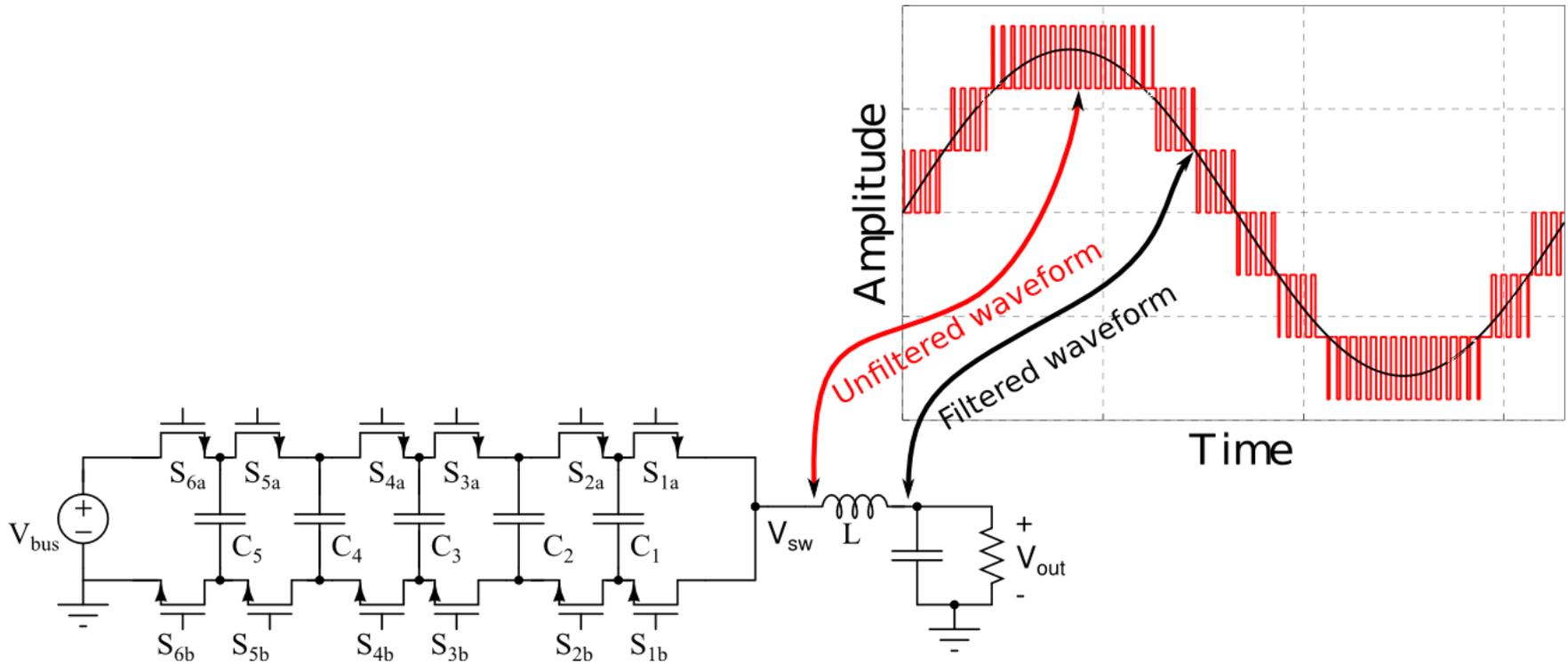
70 mJ of inductor energy storage



70 mJ of capacitor energy storage



Multi-Level Flying-Capacitor Converter



- Inductor ripple frequency: $f_{sw} \times (N - 1)$
 - Reduced ripple voltage amplitude: $V_{DC}/(N - 1)$
 - Reduced switch voltage stress: $V_{DC}/(N - 1)$
 - Heat spreading
- } Inductor reduced by $(N - 1)^2$

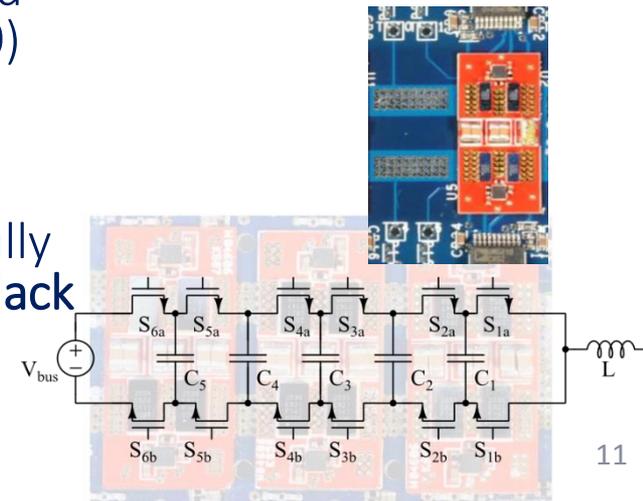
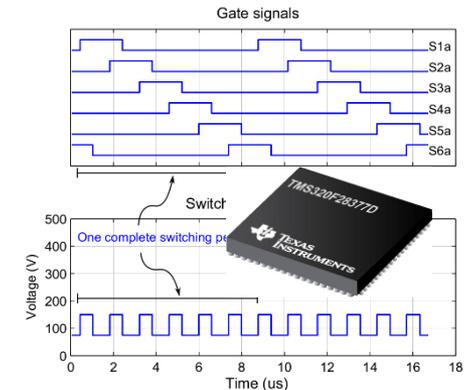
Implementation Challenges



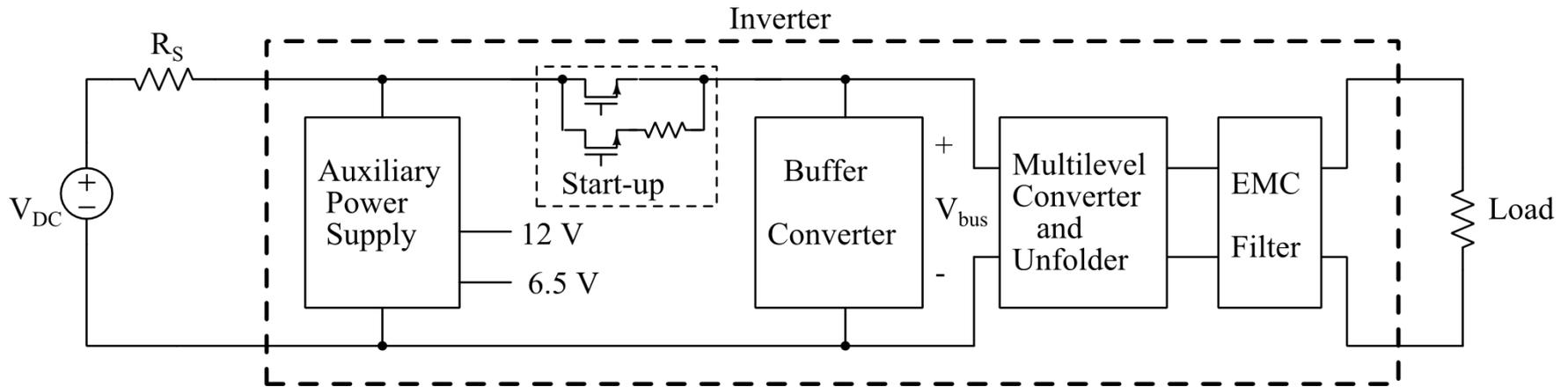
Few experimentally demonstrated examples of > 5 level flying capacitor multi-level inverter, and none switching in the 100's of kHz at kW levels.

Challenges

- Capacitor voltage balancing
 - Approach: natural balancing with phase-shifted PWM (**digital control**)
- Gate driving complexity
 - Approach: Half-bridge gate drivers (LM5113) and integrated isolated dc-dc converter (ADUM5210) (**integration**)
- Parasitic inductance
 - Approach: Integrated switching cells with carefully controlled impedance (**integration, packaging, black magic**)

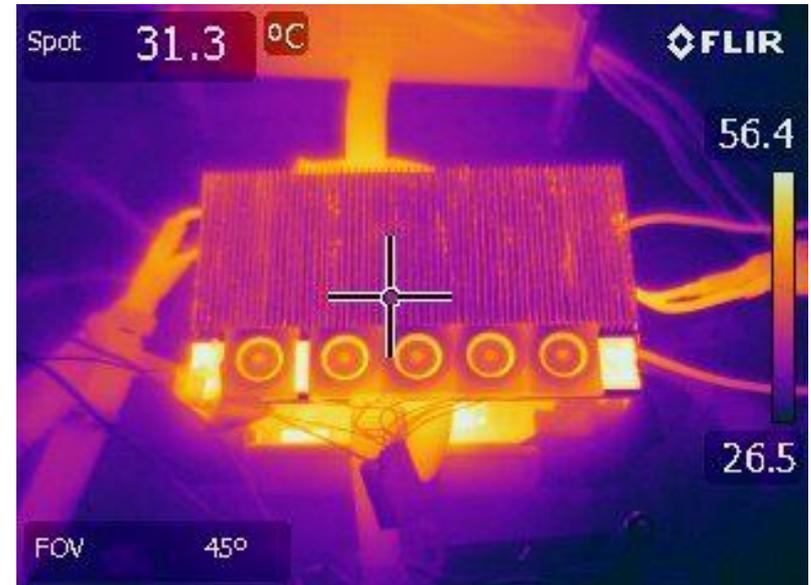
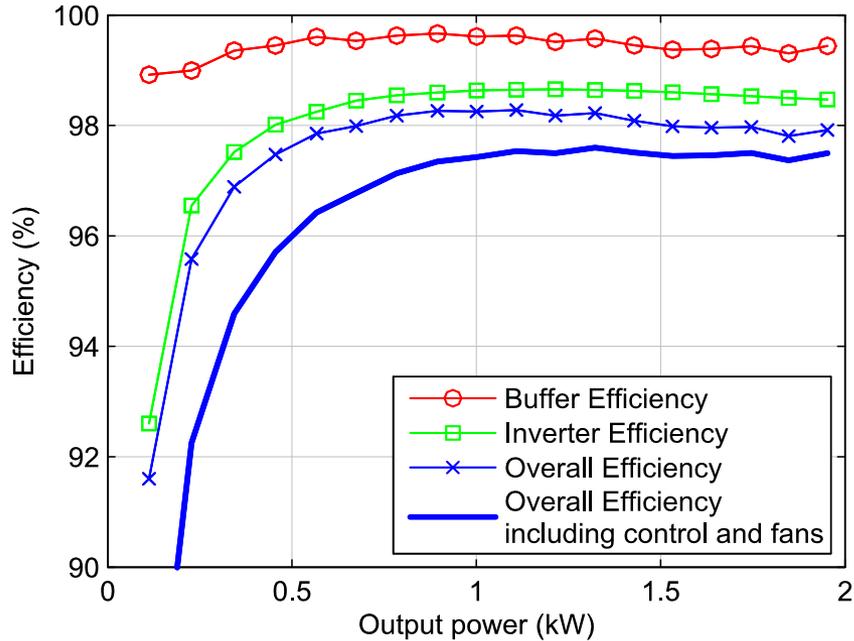
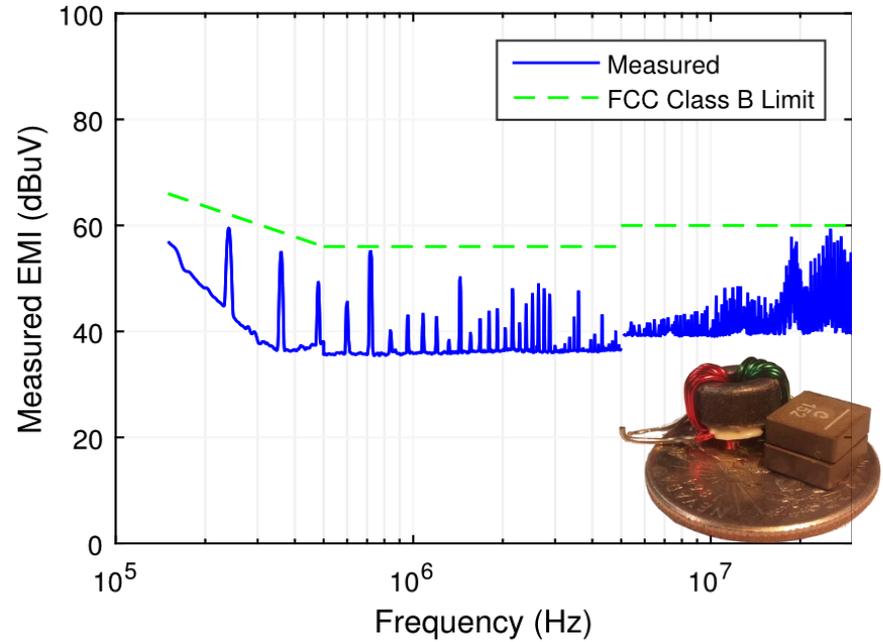
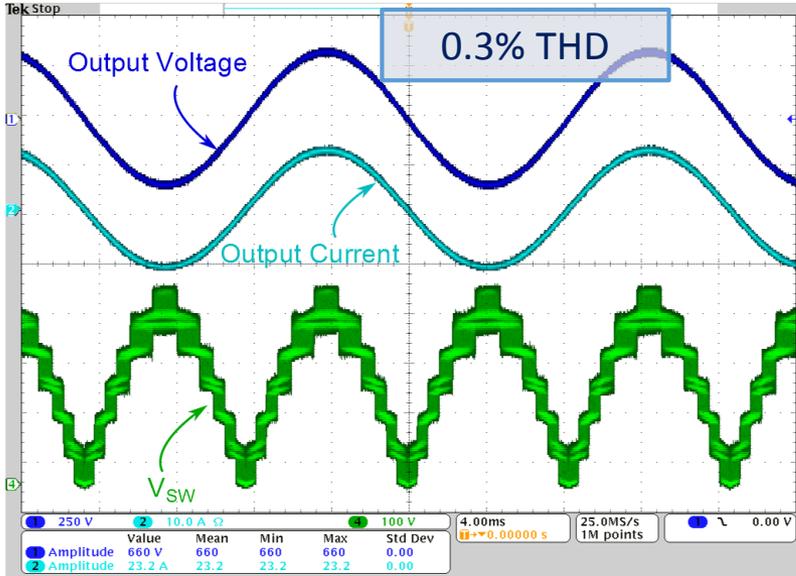


2 kW Hardware Prototype

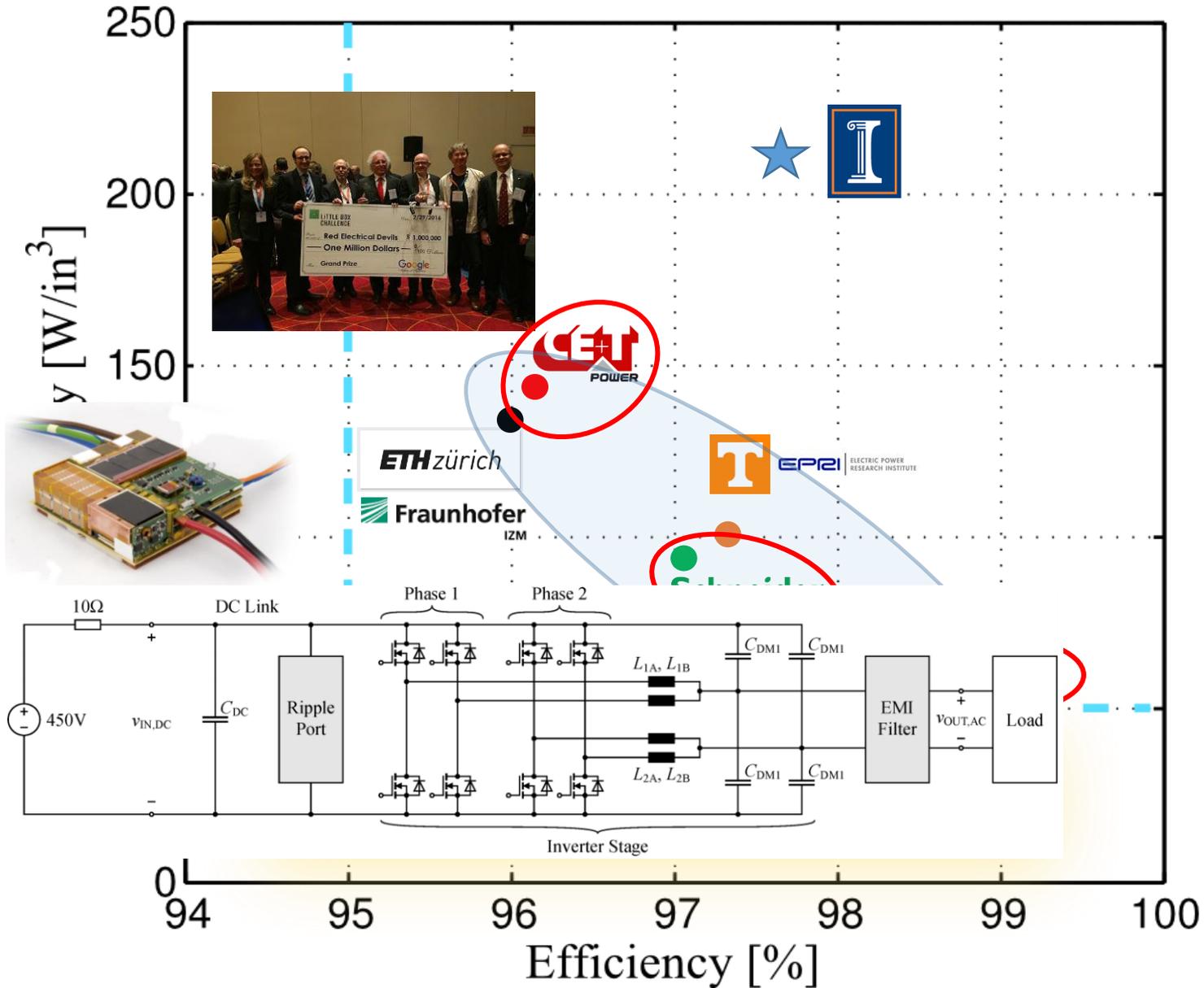


Y. Lei, C. Barth, S. Qin, W.-C. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao and R.C.N. Pilawa-Podgurski "A 2 kW, Single-Phase, 7-Level, GaN Inverter with an Active Energy Buffer Achieving 216 W/in^3 Power Density and 97.6% Peak Efficiency", IEEE Applied Power Electronics Conference, Long Beach, CA, 2016

Experimental Results



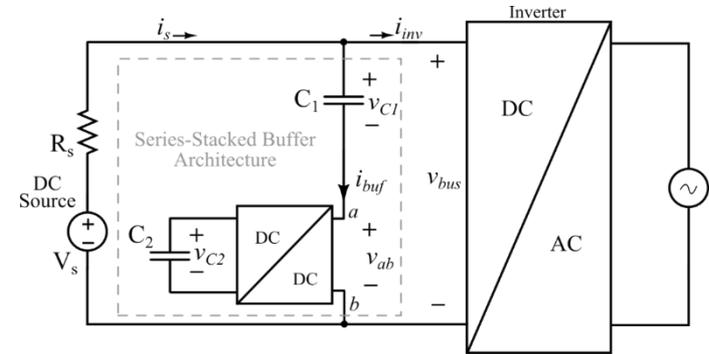
Selected Teams (efficiencies at 2 kW)



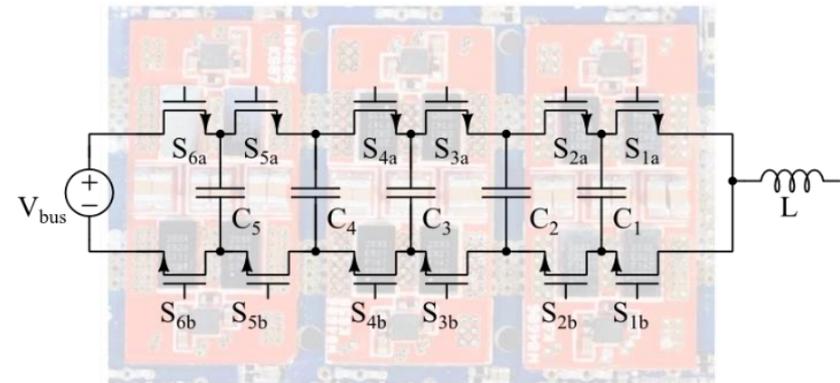
Conclusions



- Circuit topologies
 - Reduced switch stress
 - Partial power processing
 - Smaller inductor
 - Increased effective frequency
 - Decreased voltage amplitude
 - Waveform properties
 - Reduced EMI generation
- Control techniques
 - Leverage digital advances
- Integration and packaging
 - Parasitic inductance
 - Thermal management



Unlikely to discover entirely
“new” topologies



Final note: Our design had one of the lowest switching frequencies
of any finalist, but the highest power density

Acknowledgments – The Pilawa Group

