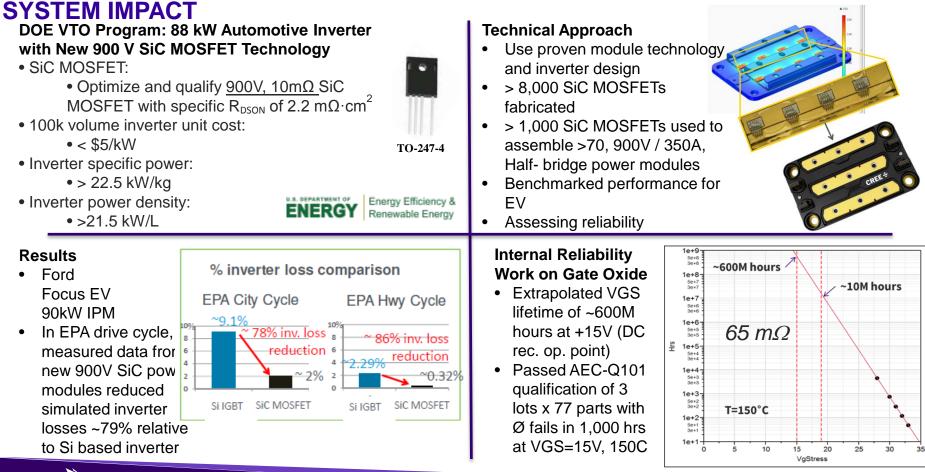


Advanced SiC Devices and Modules Address System Challenges

Dr. Ty McNutt September 13, 2016

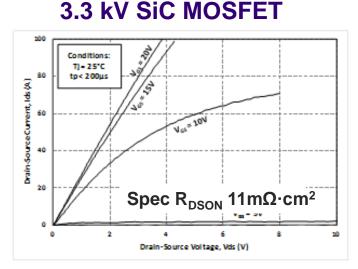
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900 V – 1700 V PRE-RELEASED & COMMERCIAL MOSFETs HAVE PROVEN



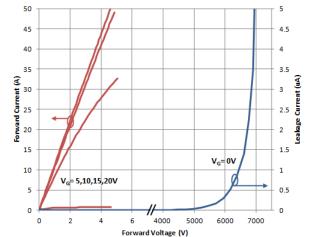


PRE-RELEASED 3.3kV & 6.5 kV GEN3 SiC MOSFETs ENABLE SYSTEM BOM REDUCTION & f_s INCREASE



- Nominally a 40A SiC MOSFET
- R_{DSONmax} at room temp ~41m Ω
- $R_{DSONmax}$ at 90°C ~98m Ω
 - all parameters subject to change without notice

6.5 kV SiC MOSFET



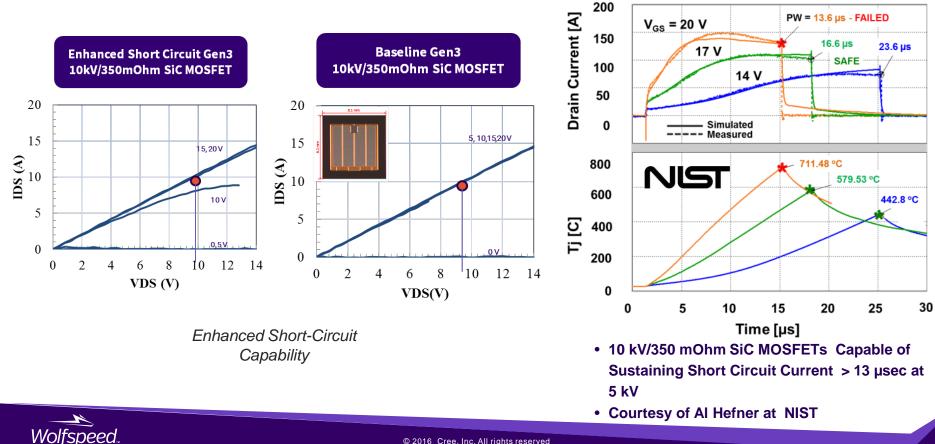
- Nominally a 20-30A SiC MOSFET
- R_{DSONmax} at room temp ${\sim}100m\Omega$
- $R_{DSONmax}$ at 90°C ~171m Ω
 - all parameters subject to change
 without notice



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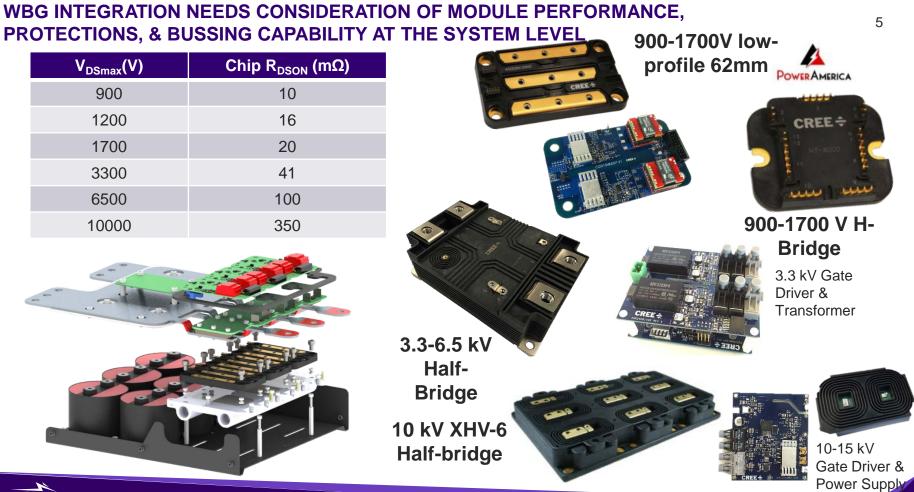
3

GEN 3 10 KV/350 m Ω SIC MOSFETS & SIMULATION/TEST OF ENHANCED SHORT CIRCUIT CAPABILITY



4

Short Circuit Voltage = 5000 V



Wolfspeed.

NEXT GENERATION MODULES NEED TO GO BEYOND LOW INDUCTANCE AND HIGH TEMPERATURE

HT-3000 Series

CAS325M12HM2 Commercial Product

Developed for dual-use with

U.S. AIR FORCE

- Equalized impedances across die
- 5 nH V+/V- Loop inductance
- High Tj capability
- Form fitting gate driver, 3-Phase Eval Kit, Full LTSpice models, Application notes...

XHV-6 10-15 kV Pre-Released Module

Developed for dual-use with



 Equalization, Low L (~15 nH), and High T can map over...

...However modules need to balance simple, low inductance bussing & keep low inductance internally

...as well as have integrated health protections to protect during fault situations

 Platform will drive cost/performance trade-off and dictate integration levels



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WORKING DIRECTLY WITH SYSTEM DESIGNERS ENABLES FULL UTILIZATION OF WBG POTENTIAL

- Clean sheet thinking
 - Topologies need to be re-considered for WBG in general
 - Advanced packaging needs developing within these topologies to ease system integration issues
 - Re-imagine what is possible by combining SiC MOSFETS, integrated packaging, and optimized topologies
 - Consider the PHEV on-board charger and Little Box Challenge Work
- Packaging technology can be optimized across power levels
 - Advanced low power packaging (<50 A) needs advancement in the advanced cooling, e.g., half bridge with <1nH inductance >>500 kHz
 - Smart medium and higher power packaging (>50A) needs integrated gate control and protections such as over I/V/T. Integrated health monitoring for robust operation under faults

ee-roliability

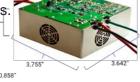
ARPA-e funded 6 kW SiC-based PHEV on-board charger

- Used Bridgeless Boost on Frontend to Eliminate Rectifier Drop & f_s Increase to Shrink Filter Size

f_s Increase to Shrink Filter Size GLBC – Used HERIC Topology

& Commercial 900 V, 65 m Ω .

- Custom FB Module for HERIC Common Source to Eliminate Common-Mode, Optimized for Xfmrless & Implements On-Board Caps.







Leading the Pack...

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