arpa·e
CHANGING WHAT'S POSSIBLE

Power Nitride Doping Innovation Offers Devices Enabling SWITCHES (PNDIODES) Program Overview

B. PROGRAM OVERVIEW

1. Summary

The PNDIODES (Power Nitride Doping Innovation Offers Devices Enabling SWITCHES) program seeks to fund transformational advances and mechanistic understanding in the process of selective area doping in the III-Nitride wide band gap (WBG) semiconductor material system and the demonstration of arbitrarily placed, reliable, contactable, and generally useable p-n junction regions that enable high-performance and reliable vertical power electronic semiconductor devices. The microscopic mechanistic understanding and transformational technologies will address the major obstacle in the fabrication of vertical GaN power electronic devices experienced by most of the teams in the ARPA-E SWITCHES (Strategies for Wide Bandgap, Inexpensive Transistors for Controlling High-Efficiency Systems) program. This challenge has been the lack of a viable GaN selective area doping or selective area epitaxial regrowth process that yields material of sufficiently high quality to enable a defect-free p-n junction on patterned GaN surfaces. Success in this area will allow further development of a revolutionary and powerful class of vertical GaN power electronic devices suitable for 1200V to 10kV broad range of applications (consumer electronics, power supplies, solar inverters, wind power, automotive, motor drives, ship propulsion, rail, and the grid).

2. Background

Electricity accounted for 40% of primary energy consumption in the United States in 2011.[1] Power electronics are projected to play a significant and growing role in the delivery of this electricity. It has been estimated that as much as 80% of electricity could pass through power electronics between generation and consumption by 2030. [2] (30% of electrical energy passed through power electronics converters in 2005.) Technical advances in power electronics promise enormous energy efficiency gains throughout the United States economy. [3]

Achieving high power conversion efficiency in these systems requires low-loss power semiconductor switches. Today's incumbent power semiconductor switch technology is silicon-based Metal Oxide Semiconductor Field Effect Transistors (MOSFET), Insulated Gate Bipolar Transistors (IGBT) and thyristors. Silicon power semiconductor devices have several important limitations:

(1) High Losses: The relatively low silicon bandgap (1.1 eV) and low critical electric field (30 V/µm) require high voltage devices to have substantial thickness. The large thickness translates to devices with high resistance and associated conduction losses.
(2) Low Switching Frequency: Silicon high voltage power MOSFETs require a large die area to keep conduction losses low. Resulting high gate capacitance and gate charge produce large peak currents and losses at high switching frequencies. Silicon IGBTs may have smaller die than MOSFETs due to utilization of minority carriers and conductivity modulation, but the relatively long lifetime of minority carriers reduces the useful switching frequency range of IGBTs.
(3) Poor High-Temperature Performance: The relatively low silicon bandgap also contributes to high intrinsic carrier concentrations in silicon-based devices, resulting in high leakage current at elevated temperatures. Temperature variation of the bipolar gain in IGBTs amplifies the leakage and limits the maximum junction temperature of many IGBTs to 125 °C.

---

[1] U.S. Energy Information Administration, *Annual Energy Review 2011* (Washington, DC: U.S. Department of Energy, 2012), http://www.eia.gov/totalenergy/data/annual/index.cfm

[2] L.M. Tolbert, et al., "Power Electronics for Distributed Energy Systems and Transmission and Distribution Applications: Assessing the Technical Needs for Utility Applications." (Oak Ridge, TN: Oak Ridge National Laboratory, 2005)

[3] "SiC and GaN electronics: Where, when and how big?" *Compound Semiconductor*, July 27, 2012, http://www.compoundsemiconductor.net/csc/features-details.php?cat=features&id=19735293

Table 1: Power Semiconductor Material Properties[4,5,6]

		Si	4H-SiC	GaN (2 DEG)	GaN (Bulk)	Diamond
Band Gap	**Eg (eV)**	1.1	3.26	3.39	3.39	5.45
Intrinsic Concentration	**n_i (cm^{-3})**	1.5×10^{10}	8.2×10^{-9}	1.9×10^{-10}	1.9×10^{-10}	1.6×10^{-27}
Electron Mobility (low)	**μ_n (cm^2/V s)**	1350	700	1000	500	1900
Electron Mobility (high)	**μ_n (cm^2/V s)**	1450	950	2000	1200	4000
Electron Saturation Velocity	**v_{sat} (10^7cm/s)**	1	2	2.5	2.5	2.7
Breakdown Electric Field	**E_{br} (MV/cm)**	0.3	2	3.3	3.5-3.75	5.6
Thermal Conductivity	**K (W/cm °K)**	1.5	4.9	1.3	2.3	20

There is great interest in developing power electronic devices using wide-bandgap (WBG) semiconductors[7,8] as they offer new opportunities for higher efficiency power semiconductor devices by circumventing the fundamental physical limits associated with silicon. The reason is illustrated by the power figure-of-merit[7] formulated as BV^2/R_{sp}, which captures the trade-off between the device specific resistance (R_{sp}) versus the device breakdown voltage (BV). For vertical unipolar devices, the theoretical specific on-resistance $R_{ON,SP}$ limits for various semiconductors are calculated from the well-known formula[9]:

$$R_{ON,SP} = \frac{4\,BV^2}{\varepsilon_S\,\mu_n\,E_C{}^3} \qquad [1]$$

where BV is the avalanche breakdown voltage, ε_S is the dielectric constant, μ_n is the majority charge carrier mobility, and E_c is the critical electric field strength at avalanche breakdown. As can be seen from equation [1] the power figure-of-merit is the denominator of this expression and can be approximated by $\sim\mu_n E_C{}^3$ which shows the power figure-of-merit scales with the cube of the critical electric field. The clear advantage of WBGs over Si can be seen in Table 1 which compares several different wide band-gap semiconductors relative to silicon. The critical electric field for Si is 0.3 MV/cm and we can estimate a value of at least 3.5 MV/cm for devices fabricated on bulk GaN and possibly as high as 3.75 MV/cm. The implication is that to achieve the same turn-on resistance and breakdown voltage, a GaN device will be a minute fraction of the area of a Si device. Since the capacitance of devices tracks area, a similar reduction in capacitance is expected (and measured). This advantage translates to faster switching, lower switching losses, higher efficiency, smaller form factor, and lighter weight power converters.

Substantial investment and technical progress has been made on WBG-based power switches over the past decade. ARPA-E has invested in WBG based power devices (SiC, GaN, & Diamond) with the Agile Delivery of Electrical Power Technologies (ADEPT) program initiated in 2010,[10] the Solar Agile Delivery of Electrical Power Technology (SOLAR ADEPT) program initiated in 2011[11], and the Strategies for Wide Bandgap, Inexpensive Transistors for Controlling High-

[4] U.K. Mishra, et al., “GaN-Based RF Power Devices and Amplifiers,” *Proceedings of the IEEE* 96, no. 3 (2008): 287-305, doi: 10.1109/JPROC.2007.911060

[5] F. Morancho, “State of the art and trends in power semiconductor devices for optimized power management,” Presentation at 40th Anniversary Meeting of LAAS-CNRS, Toulouse, France, October 2008, http://www.laas.fr/files/LAAS/40ans_LAAS-CNRS_A5-Morancho.pdf

[6] C. Mion et al., “Accurate dependence of gallium nitride thermal conductivity on dislocation density,” *Applied Physics Letters* 89, 092123 (2006), doi: 10.1063/1.2335972

[7] T.P Chow, “GaN Power Devices,” *International Symposium on Power Semiconductor Devices and ICs, Short Course*, pp. 159-186, (2008)

[8] J. Palmour, et al., “SiC Power Devices for Smart Grid Systems,” *Proceedings of IEEE International Conference on Power Electronics,* , pp. 1006-1013, (2010)

[9] K. Shenai, et al., "Optimum Semiconductors for High-Power Electronics," *IEEE Trans. On Electron Devices*, 36, 1811, (1989) doi: 10.1109/16.34247

[10] “Agile Delivery of Electrical Power Technologies,” ARPA-E, U.S. Department of Energy, released July 12, 2010, https://arpa-e.energy.gov/?q=arpa-e-programs/adept

[11] “Solar Agile Delivery of Electrical Power Technology,” ARPA-E, U.S. Department of Energy, released September 29, 2011, https://arpa-e.energy.gov/?q=arpa-e-programs/solar-adept

Efficiency Systems (SWITCHES) program initiated in 2013.[12] In addition, the Department of Defense[13] and several DOE offices including the Advanced Manufacturing Office,[14] the Office of Electricity Delivery and Energy Reliability,[15] and the Vehicle Technologies Program,[16] have helped build early U.S. leadership and bring WBG devices closer to widespread adoption. In 2014 President Barack Obama and the U.S. Department of Energy (DOE) launched PowerAmerica, a manufacturing innovation institute for next generation power electronics, to develop advanced manufacturing processes that will enable large-scale production of wide bandgap (WBG) semiconductors.[17]

To date, the majority of GaN power device development has been directed toward lateral architectures, such as high-electron mobility transistors (HEMTs), fabricated in thin layers of GaN grown on foreign substrates (including Si). Such lateral devices suffer from well-known issues such as current-collapse, dynamic on-resistance, inability to support avalanche breakdown[18], and inefficient thermal management. Many of these shortcomings arise from defects originating in the very large lattice and coefficient of thermal expansion (CTE) mismatch between GaN and the non-native substrate. If instead one could fabricate vertical architectures on lattice and CTE matched bulk GaN substrates, it might be possible to realize the material-limited potential of GaN including true avalanche-limited breakdown, increased number of die on a wafer, and more efficient thermal management leading to large device currents (> 100A) without resorting to device parallelization.

Recently, bulk GaN substrates have become more widely available, a breakthrough that is enabling vertical architectures such as GaN planar as grown p-n diodes with breakdown voltages up to 5 kV, on-state currents approaching 400A, and avalanche capability.[19,20,21]. However, the full potential of vertical architectures also requires the development of selective area doping, a breakthrough which would enable high performance vertical GaN transistors as well as merged p-n/Schottky (MPS) low turn-on-voltage diodes, and junction termination extension structures (p-type GaN rings surrounding the device perimeter) for edge termination of vertical GaN devices. In GaN, however, selective area p-type doping has proved elusive, because the most obvious approach, laterally patterned ion implantation and activation or selective area diffusion of p-type dopants (e.g. Mg, Be, Zn) has not produced p-type regions or satisfactory (i.e., equivalent to as-grown) p-n junctions. In addition, selective area etch and regrowth approaches have not resulted in sufficient electrical performance to be useful in power electronic applications. Namely, junction leakage currents have been large, breakdown voltages much lower than expected, and avalanche breakdown ruggedness not convincingly demonstrated. The microscopic mechanistic understanding for the poor electrical performance to date is incomplete or non-existent. The presence of nitrogen vacancies, interface trap states, and Si-segregation are some of the culprits proposed but never decisively proven.[22]

C. PROGRAM OBJECTIVES

This program seeks to fund transformational advances in the process of selective area doping based on mechanistic understanding in the III-Nitride wide band gap (WBG) semiconductor material system and the demonstration of randomly placed, reliable, contactable, and generally useable p-n junction regions that enable high-performance and reliable vertical

---

[12] "Strategies for Wide Bandgap, Inexpensive Transistors for Controlling High-Efficiency Systems," ARPA-E, U.S. Department of Energy, released October 21, 2013, https://arpa-e.energy.gov/?q=arpa-e-programs/switches

[13] "DARPA Sets Tough Goals For The Wide-Bandgap Community," *Compound Semiconductor*, November 8, 2002, http://compoundsemiconductor.net/csc/features-details.php?id=11332

[14] Office of Energy Efficiency and Renewable Energy, Advanced Manufacturing Office, "Wide Bandgap Semiconductor for Clean Energy Workshop: Summary Report," (Washington, DC: U.S. Department of Energy, 2012), http://www1.eere.energy.gov/manufacturing/rd/pdfs/wbg_2012_workshop_summary_report.pdf

[15] Office of Electricity Delivery and Energy Reliability, *Power Electronics Research and Development Program Plan,* April 2011 (Washington, DC: U.S. Department of Energy), http://energy.gov/sites/prod/files/oeprod/DocumentsandMedia/OE_Power_Electronics_Program_Plan_April_2011.pdf

[16] Office of Energy Efficiency and Renewable Energy, Vehicle Technologies Program, *Multi-Year Program Plan 2011-2015,* December 2010 (Washington, DC: U.S. Department of Energy), http://www1.eere.energy.gov/vehiclesandfuels/pdfs/program/vt_mypp_2011-2015.pdf

[17] PowerAmerica, 2014, https://www.poweramericainstitute.org/

[18] E. Zanoni, et al., "AlGaN/GaN-Based HEMTs Failure Physics and Reliability: Mechanisms Affecting Gate Edge and Schottky Junction," *IEEE Trans. on Electron Devices*, 60, pp. 3119-3131 (2013) doi: 10.1109/TED.2013.2271954

[19] Y. Hatakeyama, et al., "Over 3.0 GW/cm2 Figure-of-Merit GaN p-n Junction Diodes on Free-Standing GaN Substrates," *IEEE Electron Device Lett.*, 32, pp. 1674-1676 (2011)

[20] Y. Saitoh, et al. "Extremely Low On-Resistance and High Breakdown Voltage Observed in Vertical GaN Schottky Barrier Diodes with High-Mobility Drift Layers on Low-Dislocation-Density GaN Substrates," *Applied Physics Express*, 081001, pp. 1-3, (2010)

[21] I.C. Kizilyalli, et al., "Vertical Power p-n Diodes Based on Bulk GaN," *IEEE Trans. on Electron Devices*, 62, pp. 414-422, (2015)

[22] M. Azize, et al., "Inhibition of interface pollution in AlGaN/GaN HEMT structures regrown on semi-insulating GaN templates," *Journal of Crystal Growth* 299, pp. 103–108, (2007)

power electronic semiconductor devices. These transformational technologies will address the major obstacle in the fabrication of vertical GaN power electronic devices experienced by most of the teams in the ARPA-E SWITCHES program, namely, the lack of a viable GaN selective area doping or selective area epitaxial regrowth process that yields material of sufficiently high quality to enable a defect-free p-n junction on patterned GaN surfaces.

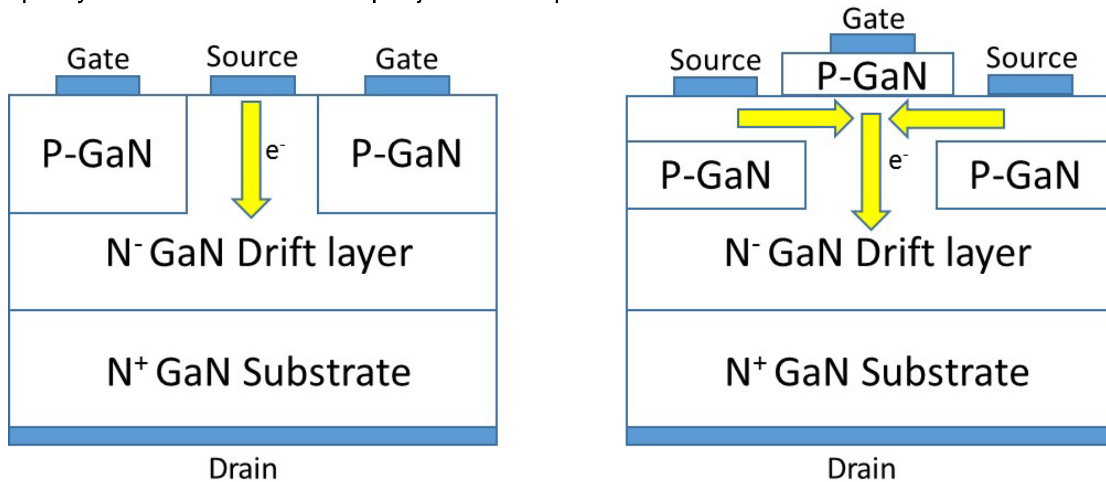

Figure 1: Two possible FET topologies. The arrows indicate the direction of electron flow.

The objective of the program can be illustrated by the two vertical transistor (switch) structures shown in Figure 1. The structure on the left is a purely vertical junction field-effect transistor (JFET) while the structure on the right has a lateral device channel along with a vertical drift region. In both structures, electrons flow from the source (top) to the drain (bottom) through the channel and drift region, and the electron flow is modulated by applying a voltage on the p-type GaN gate regions. Note that, in order to take full advantage of the high critical electric field for the onset of avalanche breakdown in GaN, it is essential to manage the electric field at the edge of the device using an edge termination to spread the potential applied to the top contacts (source and gate) over a distance which is greater than the drift region thickness. Furthermore, p-n junctions are required for avalanche ruggedness.

Both structures are difficult to fabricate. The structure on the left of Figure 1, the vertical JFET, requires selective doping of p-type regions in an n-type layer (or vice versa) while the structure on the right of Figure 1, the lateral/vertical FET, requires buried p-type GaN regions in and below the n-type channel. The typical selective area doping methods used in other semiconductor materials such as laterally patterned ion implantation and activation or selective area diffusion of dopants have not been successful in GaN to date since the low thermal stability of GaN makes the high temperature processing required for diffusion or activation in these techniques difficult.[23,24] One method more commonly used in GaN to fabricate these structures is to etch the GaN in the desired regions followed by selective area growth by MOCVD with the desired doping type.[25] However, typically the performance of devices fabricated in this method are poor with low breakdown voltage and unreliable device operation. This is thought to be due to defects at the p-n junction interfaces and large generation-recombination currents along the channel regions. The problem is further complicated with the regrowth processes which takes place along different crystal planes, such as the c-, a-, or m-direction, which is a not well understood process. In summary, the most significant barrier to viability for vertical GaN power electronics, as observed by many of the teams in the SWITCHES program, is the lack of a reliable selective area doping or selective area epitaxial regrowth process for GaN that yields material of sufficiently high quality to enable a defect-free p-n junction on patterned GaN surfaces.

Analysis and characterization of the relationships among processing, defect structure and device performance in selectively doped p-n junctions is required to fully understand and overcome the limitations of the commonly used selective area doping processes in GaN. This should be focused on developing mechanistic understanding in the areas of dopant incorporation, dopant activation, dopant diffusion, and crystal imperfections near the selective area doping interface. Powerful characterization techniques such as transmission electron microscopy, electron paramagnetic resonance, atom probe

[23] C. Ronning, et al., "Ion implantation into gallium nitride," *Physics Reports*, 351, pp. 349-385 (2001), doi: 10.1016/S0370-1573(00)00142-3

[24] O. Madelung, et al., "gallium nitride (GaN), solubility and diffusion of impurities," *Landolt-Börnstein - Group III Condensed Matter,* 41A2b, pp 1-2, (2003), doi: 10.1007/10860305_19

[25] S. Chowdhury, et al., "Current status and scope of gallium nitride-based vertical transistors for high-power electronics application," *Semiconductor Science and Technology*, 28, pp. 074014 (2013), doi: 10.1088/0268-1242/28/7/074014

tomography, Rutherford backscattering spectrometry/channeling, cathodoluminescence, and photoluminescence are available to characterize the selectively doped p-n junctions and investigate defects (point defects, dislocations, etc.) and impurities that result from the selective doping process. To achieve program goals, these measurements must be closely correlated with detailed electrical characterization using techniques such as I-V, C-V, and deep-level transient spectroscopy. Such coordinated analysis is an essential component of development of novel selective doping processes that eliminate or passivate those impurities, defects, dislocations, and vacancies that have been identified as performance limiting.

At the end of the PNDIODES program ARPA-E expects a mechanistic understanding of the relationship between processing methods and performance for selective area doping in GaN and the demonstration of randomly placed, reliable, contactable, and generally useable p-n junction regions by selective area doping to supplement the ARPA-E SWITCHES program. The Department of Energy and Department of Defense have identified power electronics based on wide-bandgap semiconductors as a major area of concern for energy efficiency and the reduction in size and weight, as well as improvement in the reliability of power conversion systems. Success would offer a valuable and innovative solution for research, development, and commercialization of vertical GaN power electronic devices.

D. TECHNICAL PERFORMANCE TARGETS

The primary goal of the program is to demonstrate or provide a pathway based on fundamental science to fabricating high quality randomly placed, reliable, contactable, and generally useable GaN p-n junctions using selective area doping of GaN. The p-n junctions need to be *electrical equivalent* to as-grown state-of-the-art (SOA) p-n junctions. The technical targets for the program are listed in Table 2. These targets are consistent with state-of-the-art p-n junctions.
Applicants are required to demonstrate how the p-n junctions will meet technical targets 1.1–1.9 in two stages:

- At the end of the first stage, p-n junctions that meet the technical targets 1.1–1.9 must be demonstrated using the selective doping process to dope a single layer adjacent to a layer of an opposite doping type to form a planar p-n junction similar to an as-grown p-n junction.
- By the end of the project period, p-n junctions that meet the technical targets 1.1–1.9 must be demonstrated using randomly or geometrically placed selectively doped regions inside and adjacent to a layer of an opposite doping type to form embedded p-n junctions giving the p-n junction vertical depth.

In both stages the p-n junctions must be demonstrated using power device appropriate dimensions and a die size >0.5mm^2. Appropriate edge termination management of the p-n junctions will be critical in successfully meeting these technical targets.

Table 2: TECHNICAL TARGETS

ID	Category	Value
1.1	Range of Controlled Selective Doping for Holes (*p*)	$1\text{x}10^{16}$ – $4\text{x}10^{17}$ cm^{-3}
1.2	Range of Controlled Selective Doping for Electrons (*n*)	$1\text{x}10^{16}$ – $1\text{x}10^{18}$ cm^{-3}
1.3	Breakdown Voltage	>= 1200 V
1.4	Leakage Current	<= $1\text{x}10^{-9}$ A (@ 600V)
1.5	Turn-on Voltage	2.6-3.4 V
1.6	Specific R_{DSON}	< 3 mΩ·cm^2
1.7	I_{on}/ I_{off} Ratio	> 10^{10}

1.8	Avalanche Capability	No parametric shift after repetitive avalanche testing[26,27]
1.9	Surge Capability	>20A surge capability for 10μs pulse at 25°C

Applicants are also required to describe the mechanistic learning techniques associated with careful examination of the selective doped regions. Mechanistic learning includes correlating characteristics of dopant incorporation, dopant activation, dopant diffusion, and crystal imperfections near selective area doping or regrowth interfaces with the device properties. Novel techniques that measure and characterize the effect of processes for the elimination or passivation of selective area doping imperfections such as impurities, defects, dislocations, and vacancies are of interest. The characterization work must be clearly targeted toward developing actionable outcomes in addressing the goal of fabricating p-n junctions (using selective area doping techniques) that are *electrically equivalent* to as-grown p-n junctions.

ARPA-E will only select projects for award negotiations that clearly demonstrate realistic, well justified potential to meet or exceed the technical performance targets.

[26] X. Huand, et al., "Ruggedness analysis of 600V 4H-SiC JBS diodes under repetitive avalanche conditions," 27th Annual *IEEE Applied Power Electronics Conference and Exposition proceedings*, pp. 1833 – 1837, (2012), doi: 10.1109/APEC.2012.6166048

[27] O. Aktas, et al., "Avalanche Capability of Vertical GaN p-n Junctions on Bulk GaN Substrates", *IEEE Electron Device Lett*., 36, pp. 890-892 (2015), doi: 10.1109/LED.2015.2456914